Abdelhafid Boussouf University Center, Mila
Institute of Mathematics and computer science
Department of Computer Science
2nd Year Informatics

Year: 2024/2025
Module: Computer Architecture

Directed Work N° 4

Exercise 1:

Suppose a computer has 2^{16} words of main memory, and a cache of 64 blocks, where each cache block contains 32 words.

a. How many blocks of main memory are there?

b. If this cache is a direct-mapped cache, what is the format of a memory address as seen by the cache, i.e., what are the sizes of the tag, block, and word fields?

c. To which cache block will the memory reference 0xF8C9 map?

d. If this cache is fully associative, what is the format of a memory address as seen by the cache, i.e., what are the sizes of the tag and word fields?

e. To which cache block will the memory reference 0xF8C9 map?

f. If this cache is 2-way set associative, what is the format of a memory address as seen by the cache, i.e., what are the sizes of the tag, set, and word fields?

g. To which cache set and block will the memory reference 0xF8C9 map?

h. If this cache is 4-way set associative, what is the format of a memory address as seen by the cache?

i. To which cache set and block will the memory reference 0xF8C9 map?

Exercise 2:

Suppose a computer using direct mapped cache has 2^{24} bytes of byte-addressable main memory, and a cache of 128 blocks, where each cache block contains 64 bytes.

(a) How many blocks of main memory are there?

(b) What is the format of a memory address as seen by the cache, i.e., what are the sizes of the tag, block, and word fields?

(c) To which cache block will the memory address 0x01D872 map?

Exercice 3:

Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 blocks is used with this machine.

a. How is a 16-bit memory address divided into tag, block number, and word number?

b. Into what block would bytes with each of the following addresses be stored?

0001 0001 0001 1011

1100 0011 0011 0100

1101 0000 0001 1101

1010 1010 1010 1010

c. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?

Exercice 4:

Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte block size.

a. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of blocks in cache, size of tag.

b. Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of blocks in cache, size of tag.

c. Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of blocks in set, number of sets in cache, number of blocks in cache, size of tag.