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2nd Year Informatics

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Module: Computer Architecture

Directed Work N° 03

Exercise1:

1- Indicate data hazards and their type for each of the following two sequences of instructions.

a.	I1: lw $1,40($6) I2: add $6,$2,$2 I3: sw $6,50($1)	
b.	I1: lw $5,-16($5) I2: sw $5,-16($5) I3: add $5,$5,$5	

2- Assume there is no forwarding in this pipelined processor. Indicate hazards and add nop instructions to eliminate them

Exercise2:

For this problem, assume that all branches are perfectly predicted (this eliminates all control hazards) and that no delay slots are used. If we only have one memory (for both instructions and data), there is a structural hazard every time we need to fetch an instruction in the same cycle in which another instruction accesses data. To guarantee forward progress, this hazard must always be resolved in favor of the instruction that accesses data. What is the total execution time of this instruction sequence in the five-stage pipeline that only has one memory? We have seen that data hazards can be eliminated by adding nops to the code. Can you do the same with this structural hazard? Why?

	Instruction sequence
a.	lw $1, 40 ($6) beq $2, $0, Label ; Assume $2 == $0 sw $6, 50 ($2) Label: add $2, $3, $4 sw $3, 50 ($4)
b.	lw $5, -16 ($5) sw $4, -16 ($4) lw $3, -20 ($4) beq $2, $0, Label ; Assume $2 != $0 add $5, $1, $4