Abdelhafid Boussouf University Center, Mila
Institute of Mathematics and computer science
Department of Computer Science
2nd Year Informatics

Year: 2024/2025
Module: Computer Architecture

Directed Work N° 4 (suit)

Exercise 1 :

For a cache with 128-byte blocks, give the addresses of the first and last words in the block containing the following address:

1 – 0xA23847EB

2 – 0x7245E837

3 – 0xEEFABC5D

Exercise 2 :

Suppose the following sequence of references, which correspond to the memory accesses requested by the processor, in terms of word addresses, in time. The addresses are given in decimal.

temps	0	1	2	3	4	5	6	7	8	9	10
adresse	731	52	63	1255	486	725	311	493	605	511	645

- Report hits, misses, and final cache contents for a direct-mapped cache with four-word blocks and a total size of 16 words.
- Compute the hit ratio

Exercise 3 :

Consider an associative cache composed of 3 entries of 4 words of 32 bits. The memory addresses are on 8 bits.

a/ What is the size of the tag?

b/ Let the following sequence of references, which correspond to the memory accesses requested by the processor, in terms of byte addresses, in time. The addresses are given in hexadecimal.

temps	0	1	2	3	4	5	6	7	8
adresse	0F	1F	3A	0D	1E	44	0B	32	17

- Give the evolution of the cache directory and note the misses in the following two cases:

1/ the replacement policy is FIFO.

2/ the replacement policy is LRU.