Flip-flop usage:

- A flip-flop is the fundamental element of sequential logic, enabling the storage of a single bit.
- Thus, flip-flops are used to create complex sequential circuits such as counters, registers, or memories.
- By combining multiple flip-flops with the same clock signal, we can construct a sequential circuit that forms a counter or a register, there by enabling the construction of memories.

The counters

A counter is a set of n flip-flops connected together in such a way as to count, at the pace of a clock, a predetermined sequence that can have a maximum of 2^n different combinations.

The binary number stored in the flip-flops of a register is regularly incremented each time a clock pulse is applied to its input.

The counters

A binary counter is called modulo N if it can count up to N - 1; the pulse following the value N - 1 resets it to zero.

Depending on the connection mode of the flip-flops, we can distinguish two types of counters:

- ✓ asynchronous counters
- ✓ synchronous counters

The counters

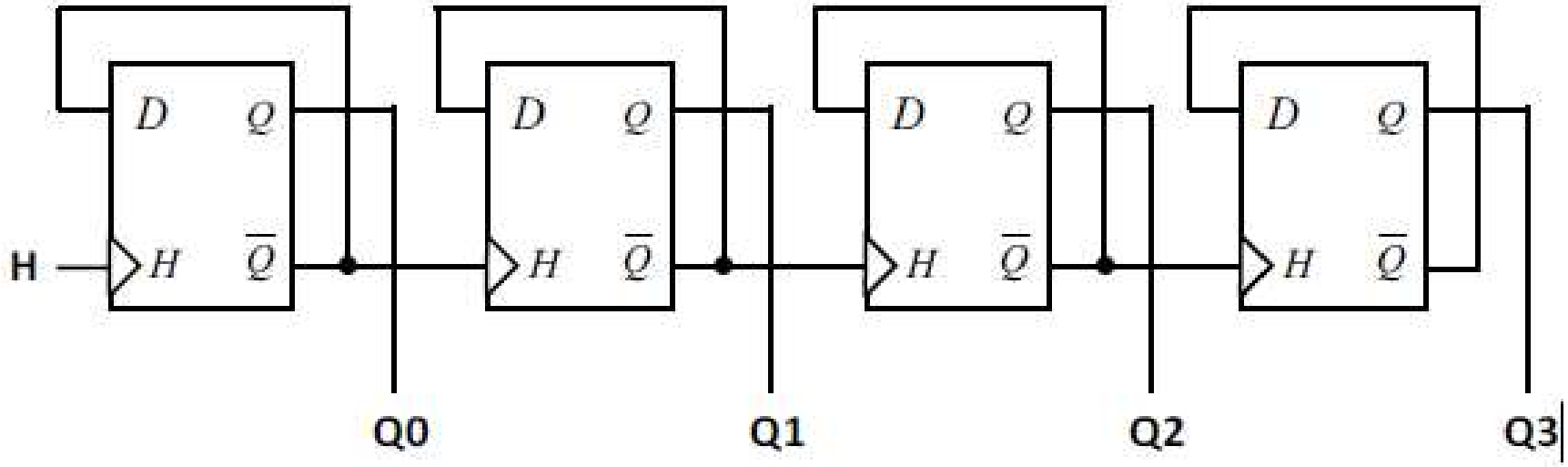
An asynchronous counter is a counter whose flip-flops are not synchronized, meaning the clock pulses of this type of counters must first pass through the first flip-flop before being able to control the second one and so on until the last flip-flop.

In this type of counters, the clock signal is only connected to the first flip-flop.

For the other flip-flops, the clock input is nothing but the output of the preceding flip-flops.

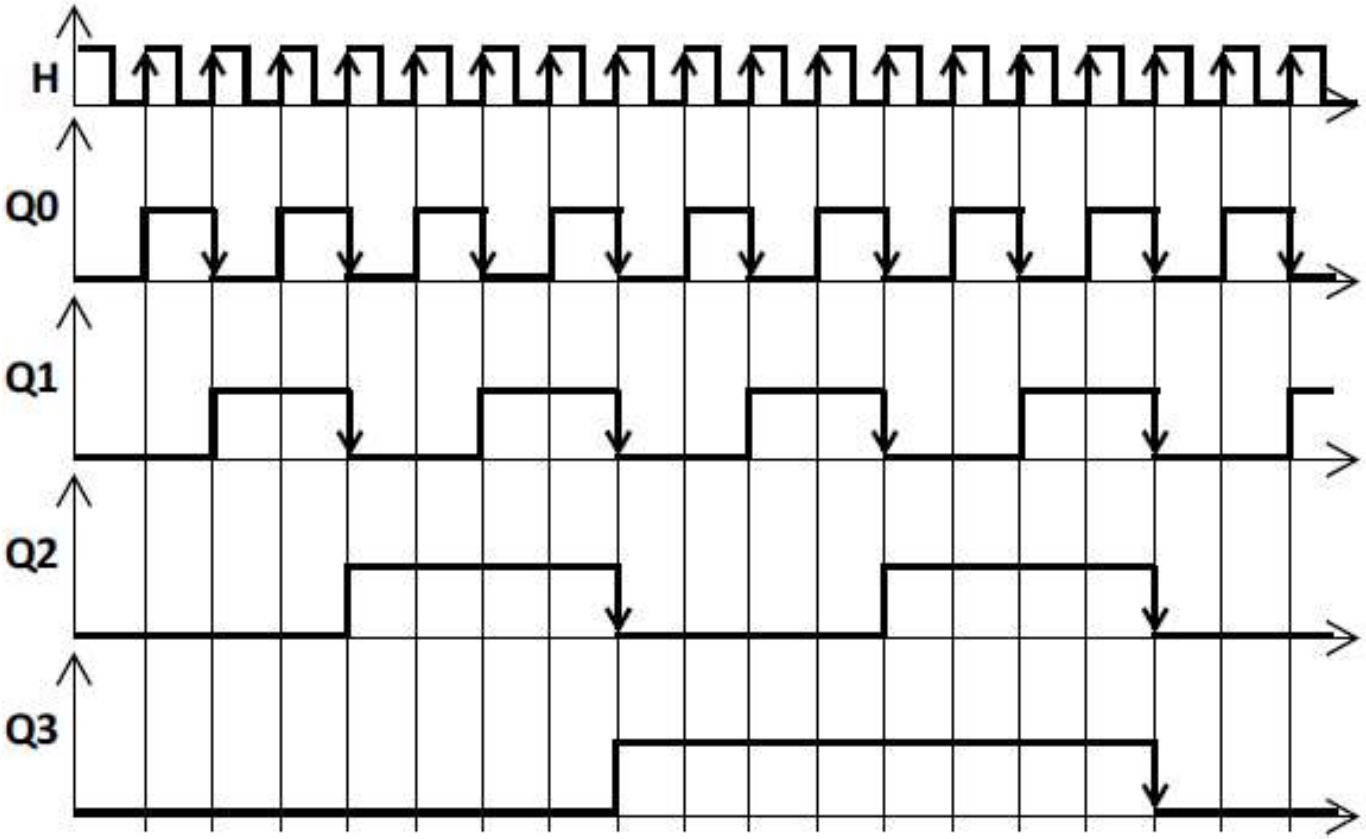
The counters

- Example: the asynchronous counter that counts from 0 to 16 will thus be given as follows:



The counters

- The corresponding timing diagram for the previous counter is given as follows:



The asynchronous counter

- Unfortunately, asynchronous counters have several disadvantages, such as:
- Limited operating speed, especially for large counters. This is due to the cumulative delay of flipping from one flip-flop to another.
- The presence of undesirable transient states on their flip-flop outputs after each increment of the counter.
- The absence of a reliable method and approach to implement counters with incomplete cycles

The asynchronous counter

- A synchronous counter is a counter whose flip-flops are synchronized to the same clock signal, meaning the clock signal of this type of counters is applied simultaneously to all the clock inputs of the different flip-flops.

- Unlike asynchronous counters, the synthesis of synchronous counters follows a well-defined approach by constructing the transition table corresponding to the state diagram of the counter.

The asynchronous counter

- summarizing

Counters

- Comprising n flip-flops interconnected by logic gates.

Counters

- Comprising n flip-flops interconnected by logic gates.
- Memorizes n bits of information

Counters

- Comprising n flip-flops interconnected by logic gates.
- Memorizes n bits of information
- Can describe a predetermined sequence of binary configurations (a sequence of binary states).

Counters

- Comprising n flip-flops interconnected by logic gates.
- Memorizes n bits of information
- Can describe a predetermined sequence of binary configurations (a sequence of binary states).
- The total number N of successive binary configurations is called the counter's modulo

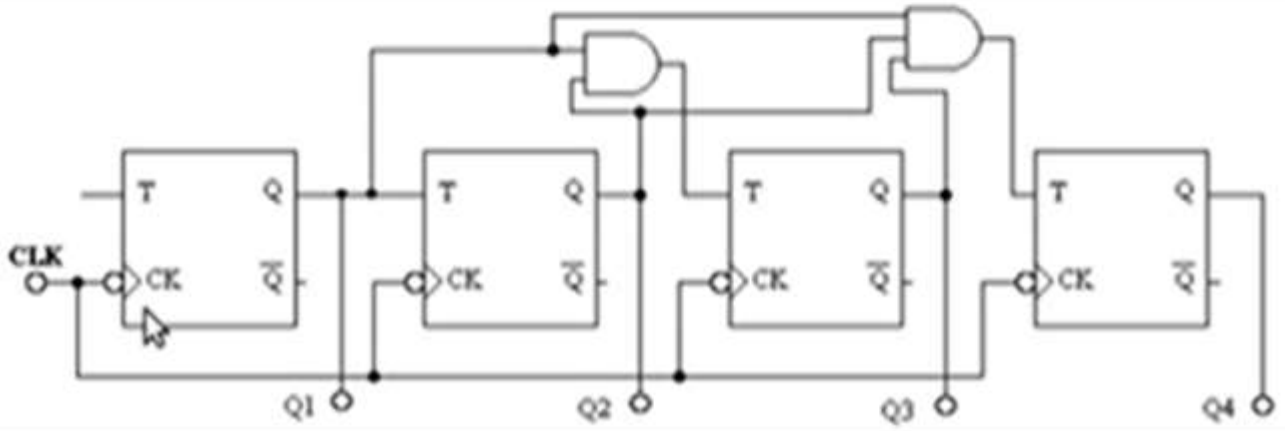
Counters

- Comprising n flip-flops interconnected by logic gates
- Memorizes n bits of information
- Can describe a predetermined sequence of binary configurations (a sequence of binary states).
- The total number N of successive binary configurations is called the counter's modulo
- We have $N \leqslant 2^n$. If $N < 2^n$ some states are never utilized.

Counters

Binary counters can be classified into two categories:
- asynchronous counters;
- synchronous counters: All flip-flops receive, in parallel, the same clock signal.

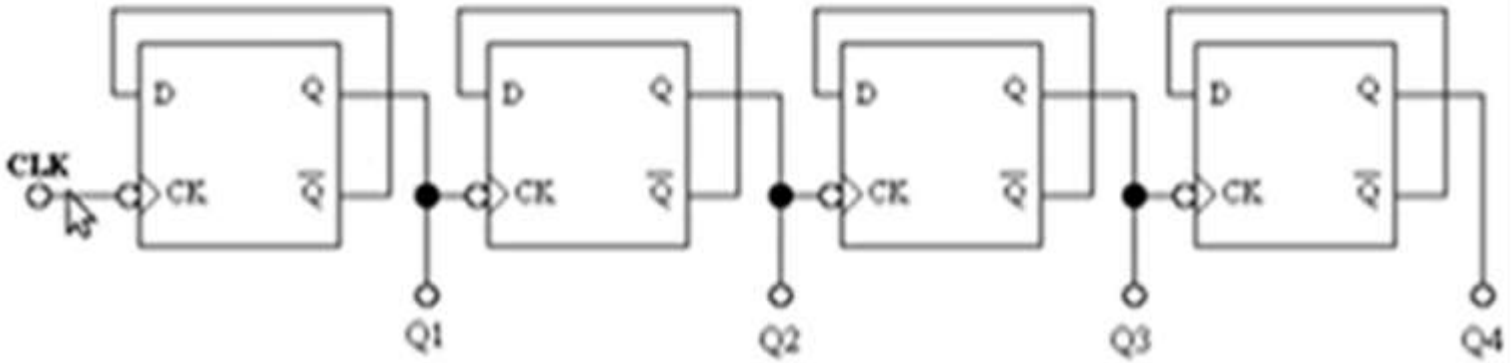
Here is an example of a synchronous counter:



Counters

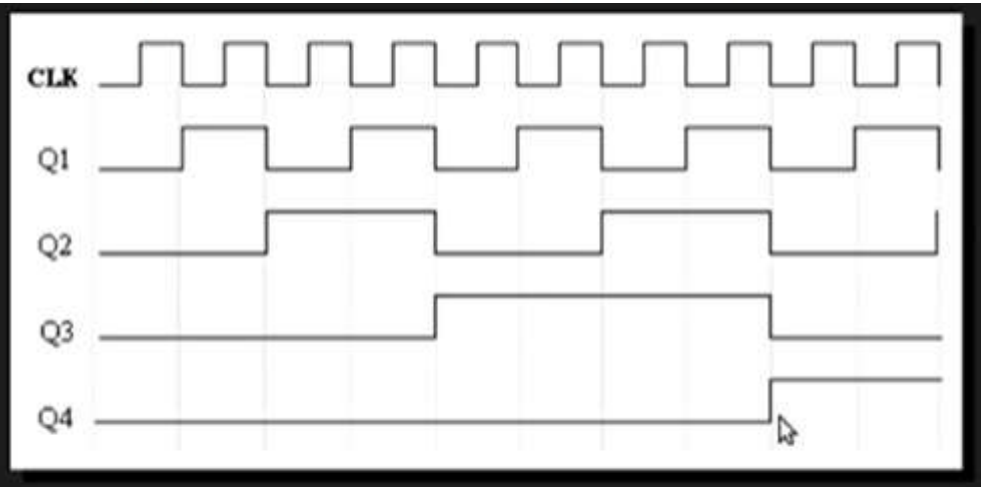
Binary counters can be classified into two categories:
- asynchronous counters;
- synchronous counters: All flip-flops receive, in parallel, the same clock signal.

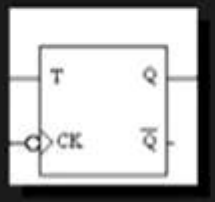
Here is an example of a synchronous counter:



Counters

To implement a counter, we rely on the frequency division property.

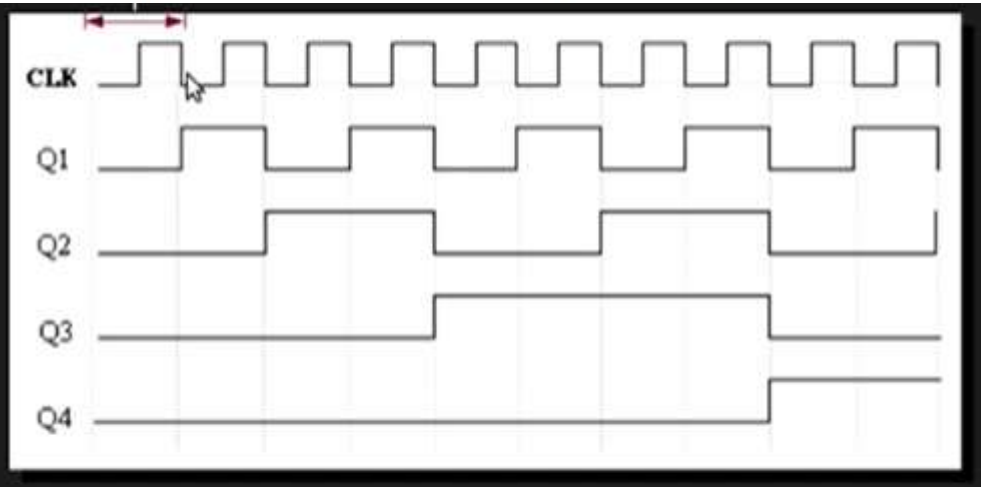


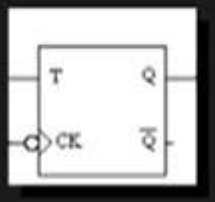


Q4	Q3	Q2	Q1

Counters

To implement a counter, we rely on the frequency division property.

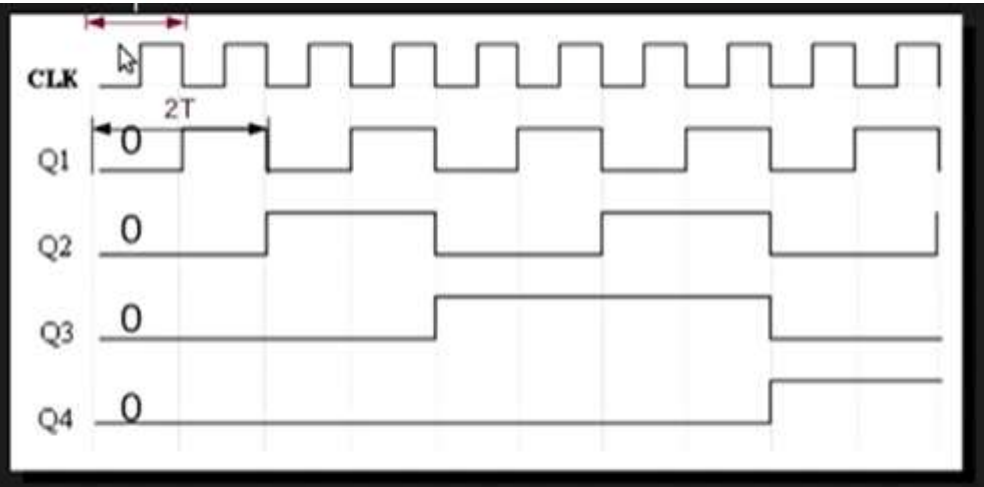


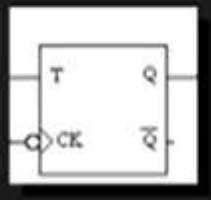


Q4	Q3	Q2	Q1

Counters

To implement a counter, we rely on the frequency division property.





Q4	Q3	Q2	Q1

Asynchronous counters

- Comprised of n J-K flip-flops operating in T mode (meaning that the J and K inputs are connected to the same signal).

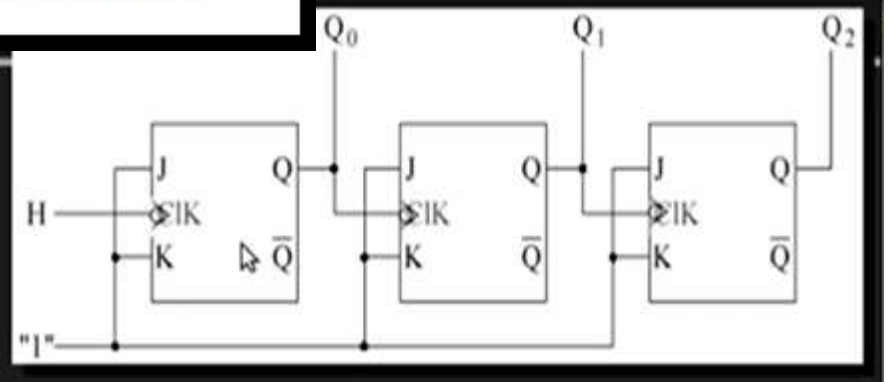
Asynchronous counters

- Comprised of n J-K flip-flops operating in T mode (meaning that the J and K inputs are connected to the same signal).
- The clock signal is only received at the first stage (LSB flip-flop: Least Significant Bit).

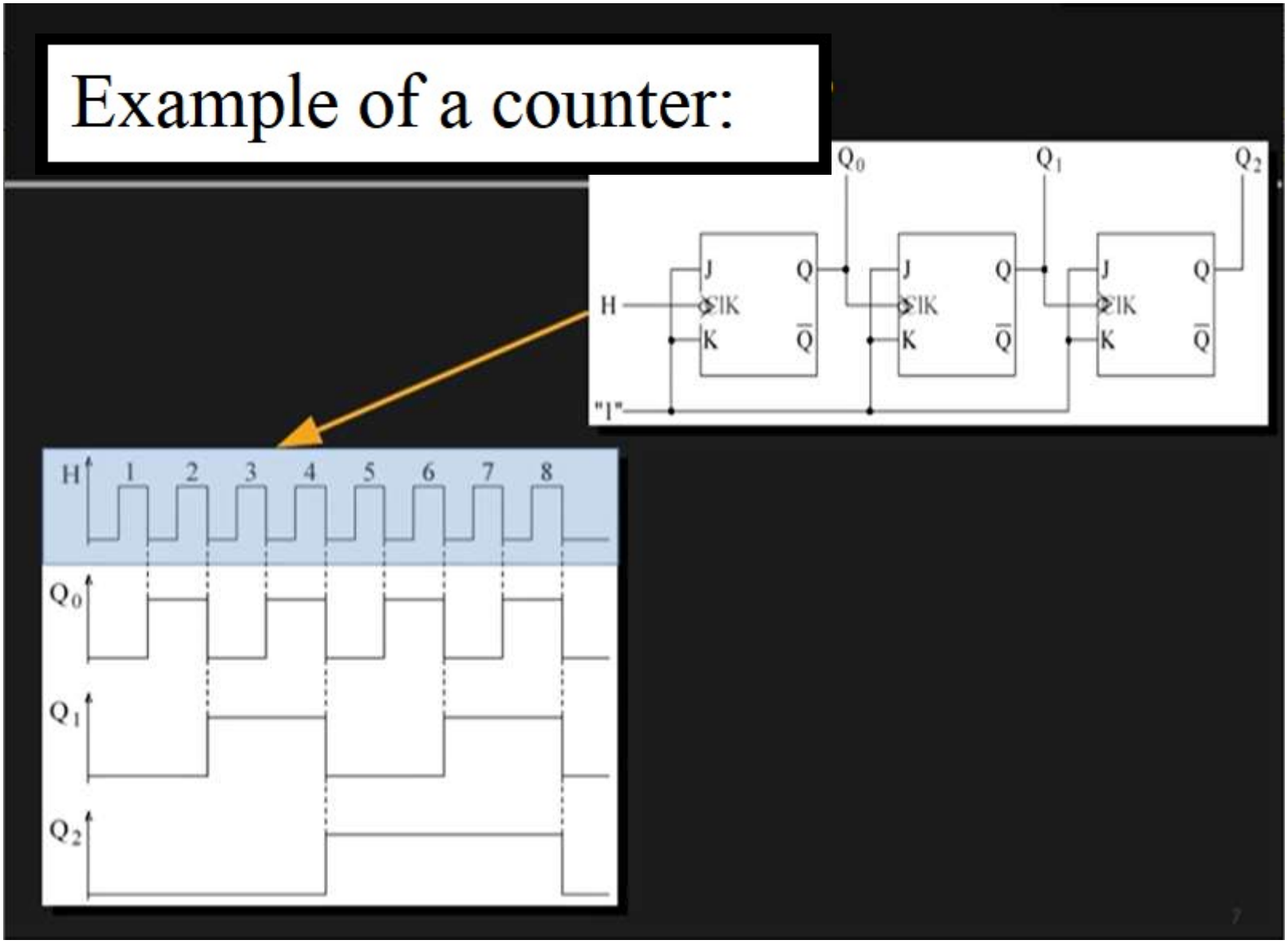
Asynchronous counters

- Comprised of n J-K flip-flops operating in T mode (meaning that the J and K inputs are connected to the same signal).
- The clock signal is only received at the first stage (LSB flip-flop: Least Significant Bit).
- For each of the other flip-flops, the clock signal is provided by an output of the flip-flop of the immediately lower rank.

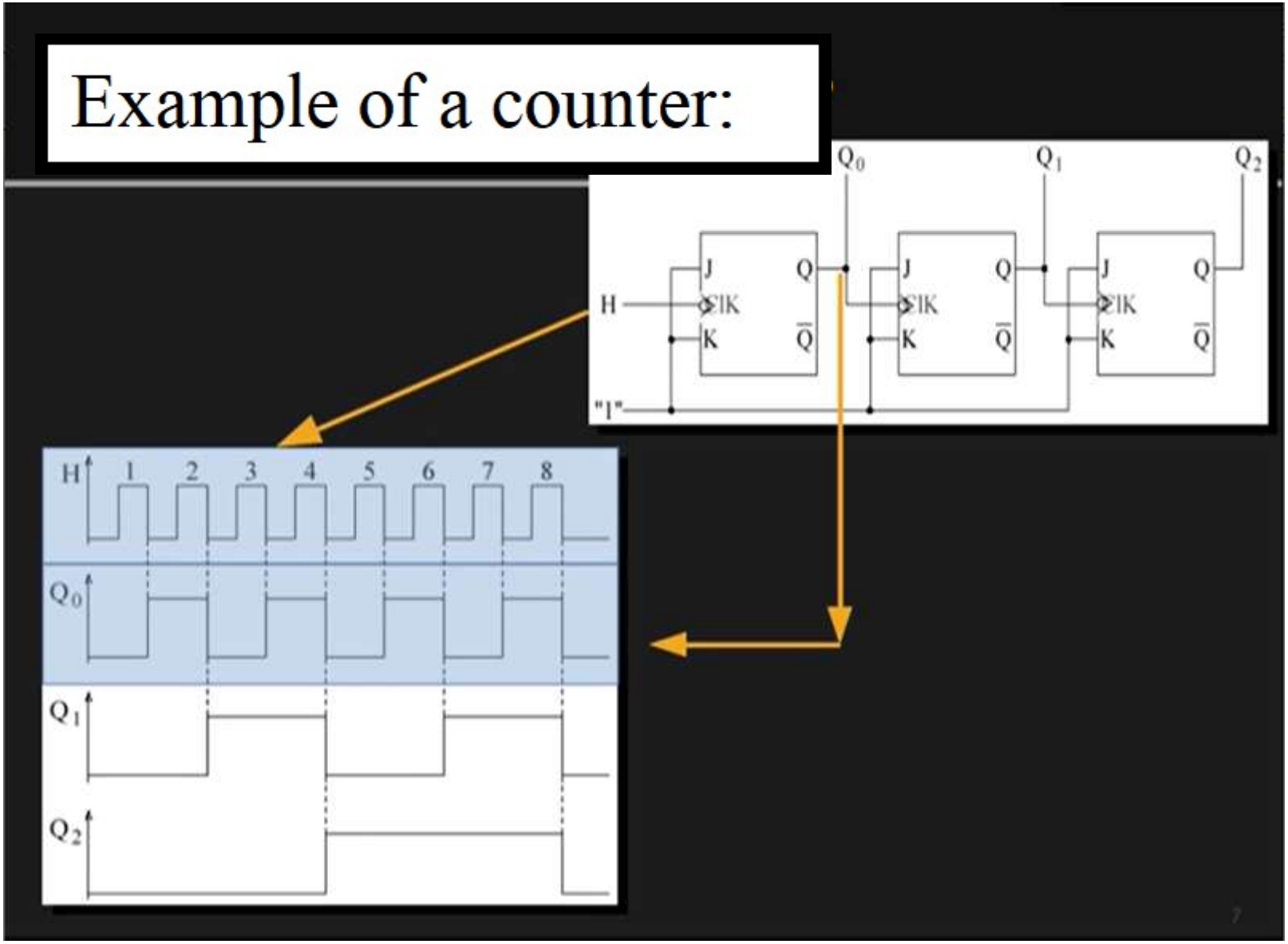
Example of a counter:



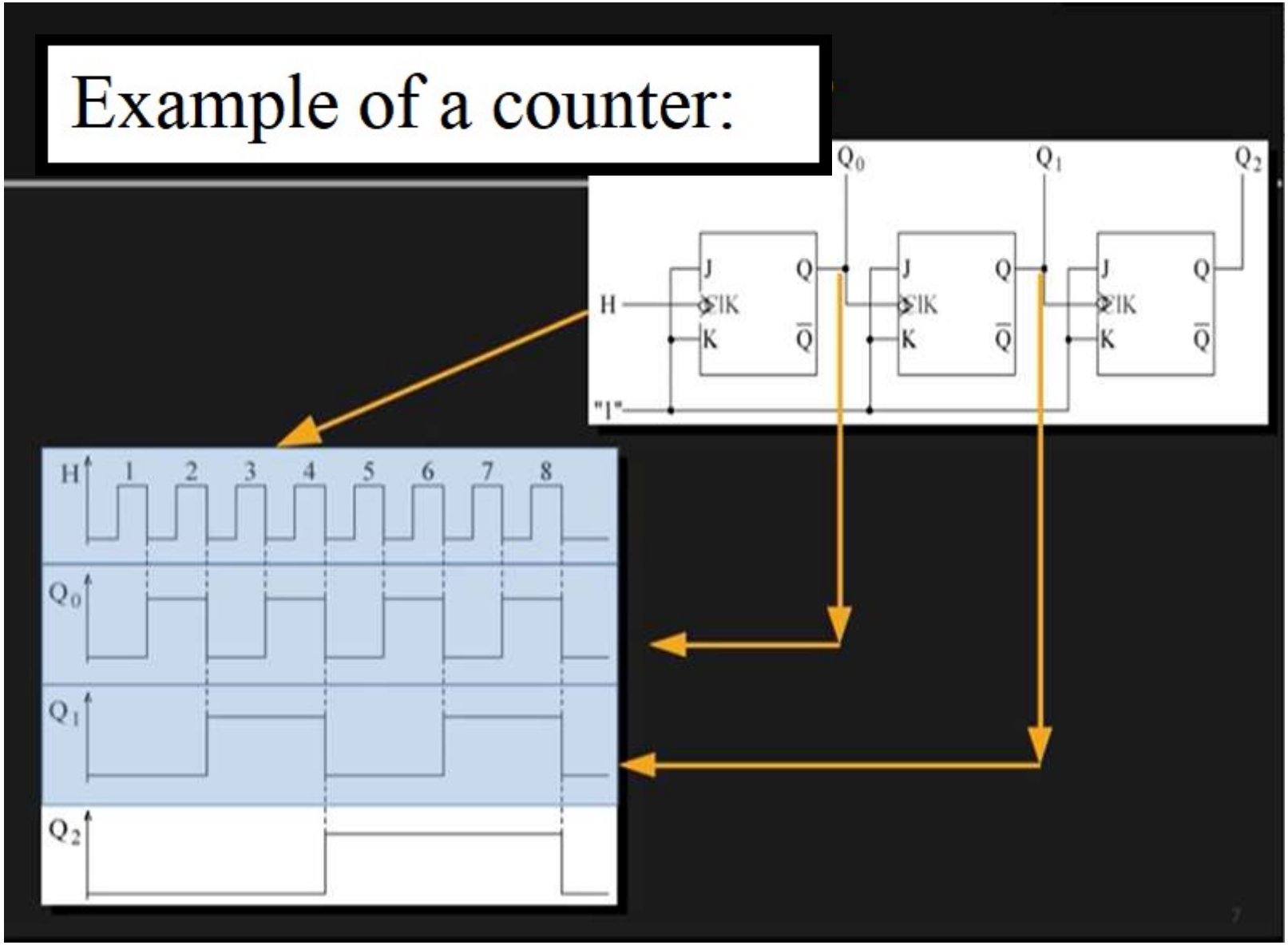
Example of a counter:



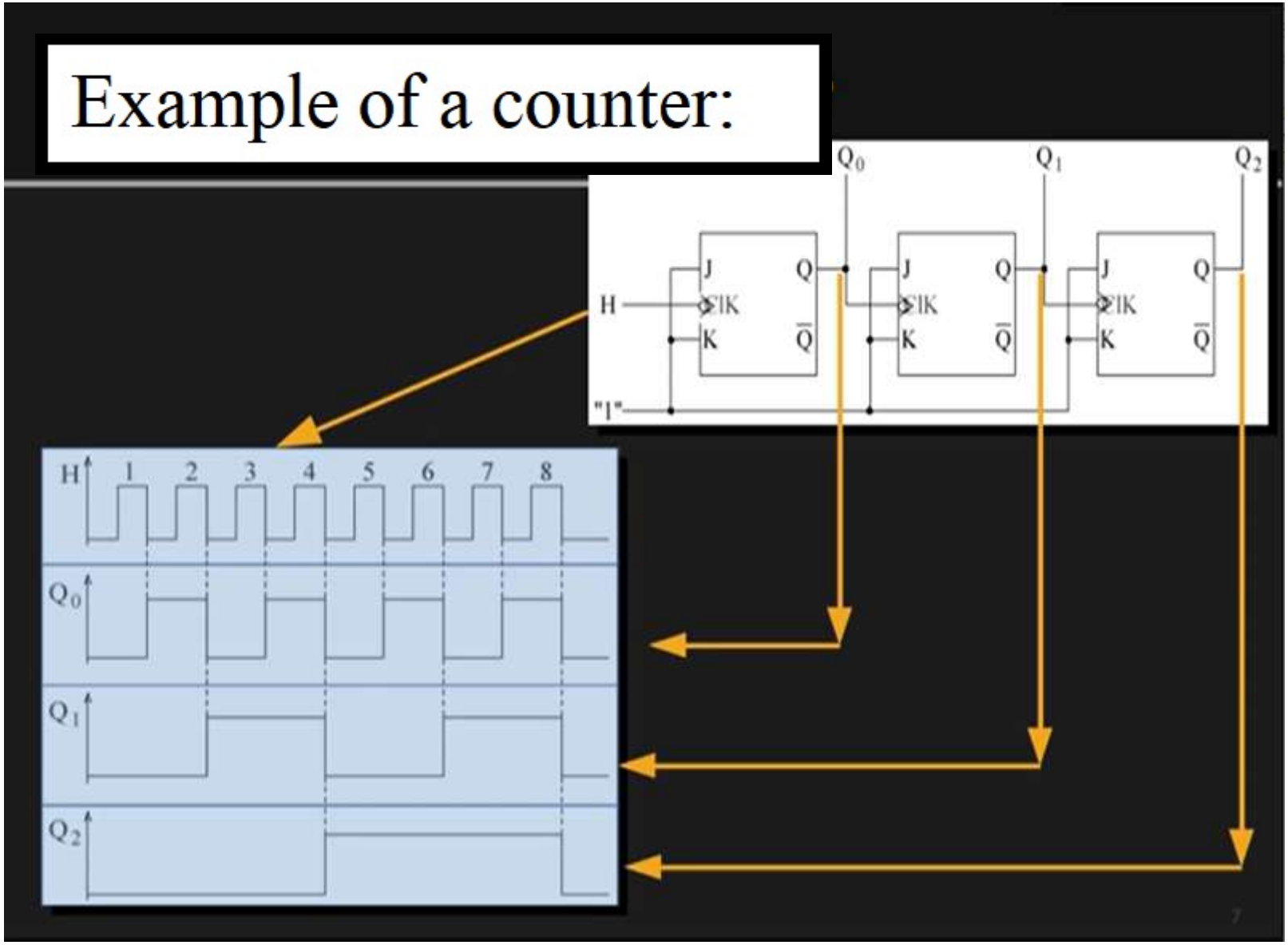
Example of a counter:



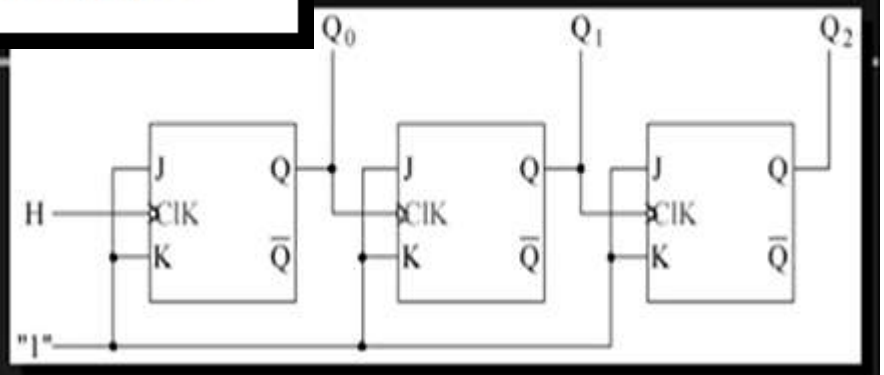
Example of a counter:

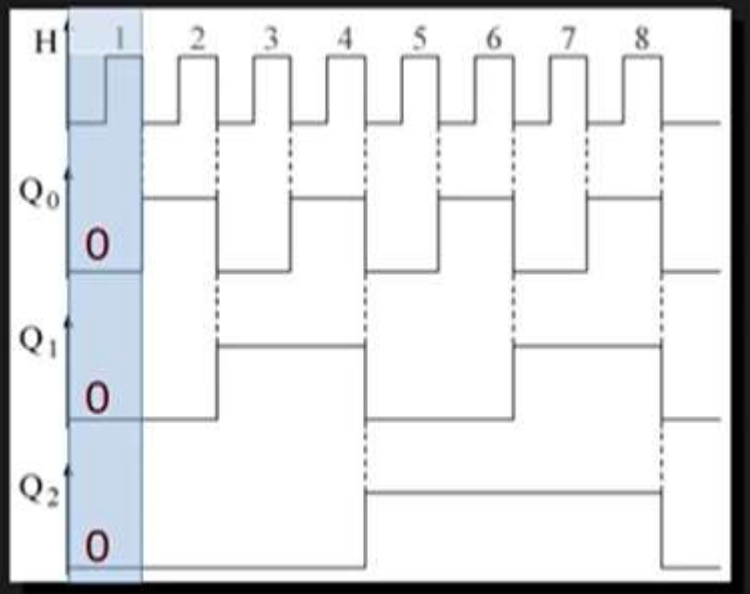


Example of a counter:

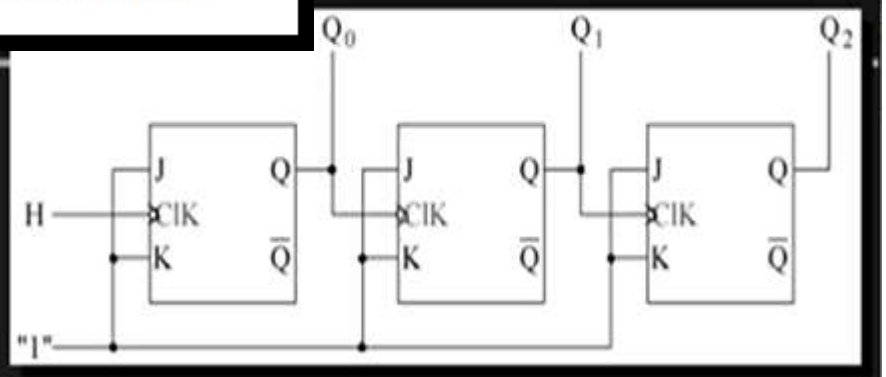


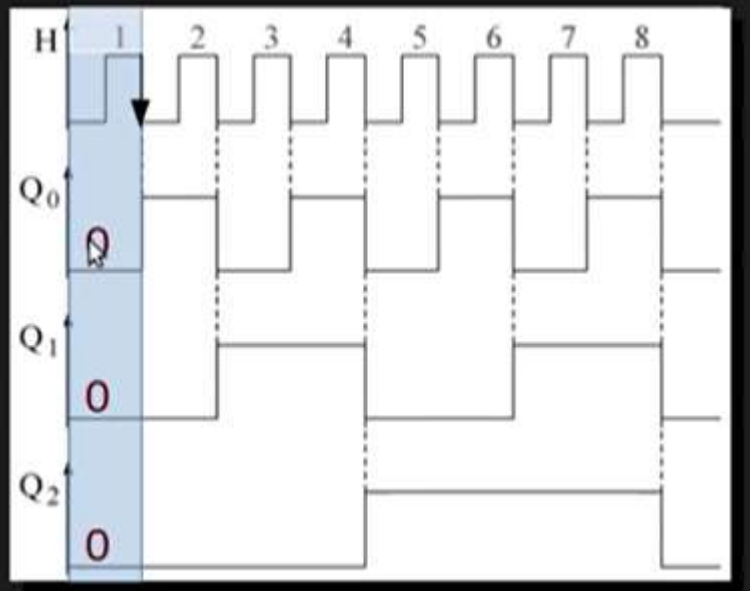
Example of a counter:



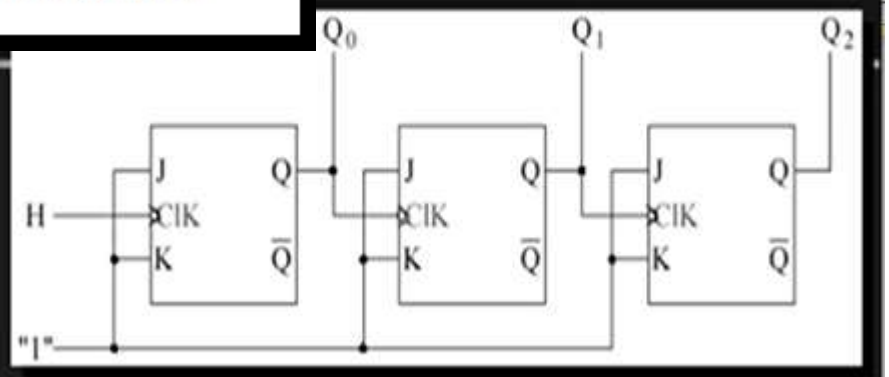


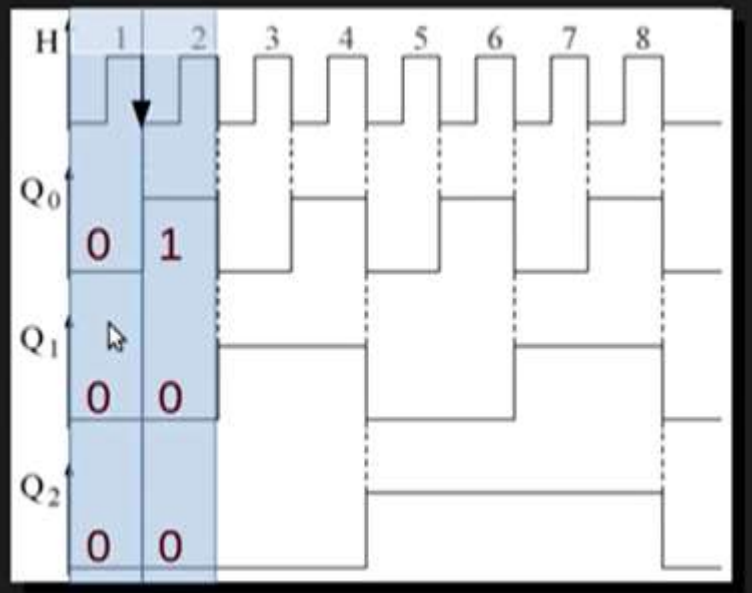
Example of a counter:



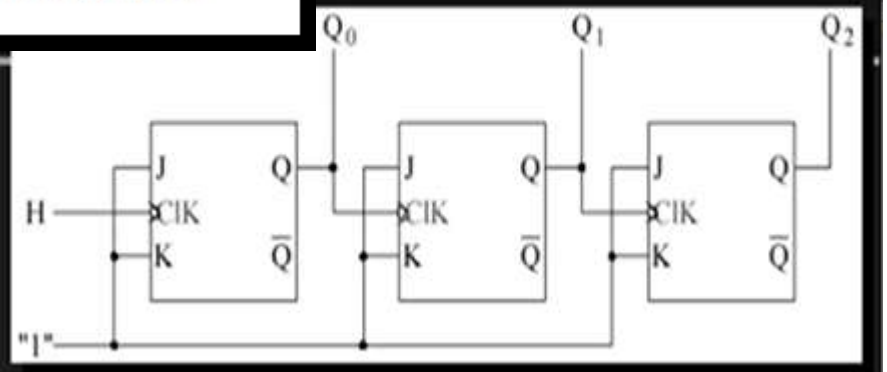


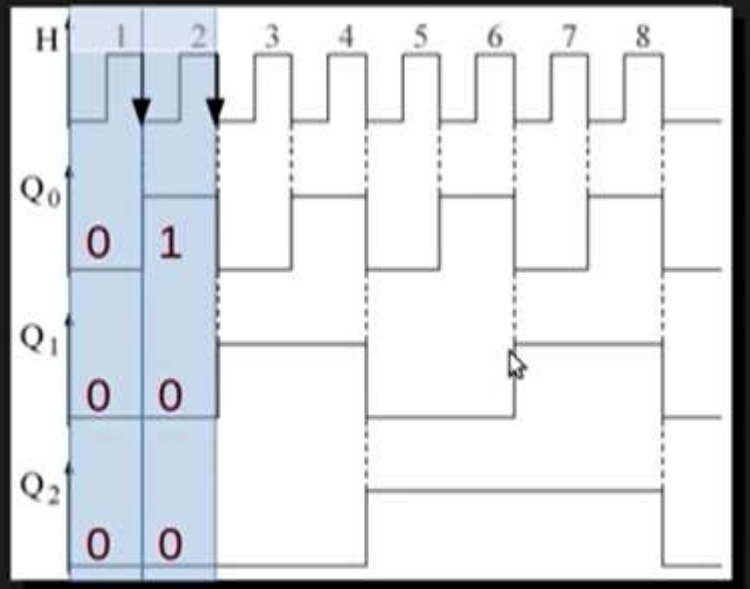
Example of a counter:



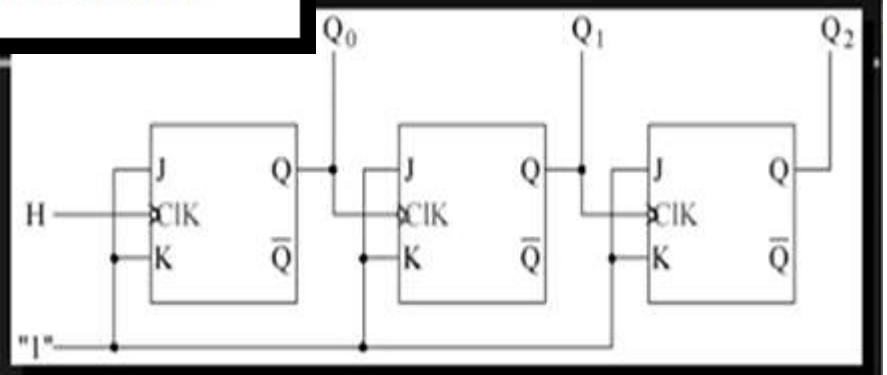


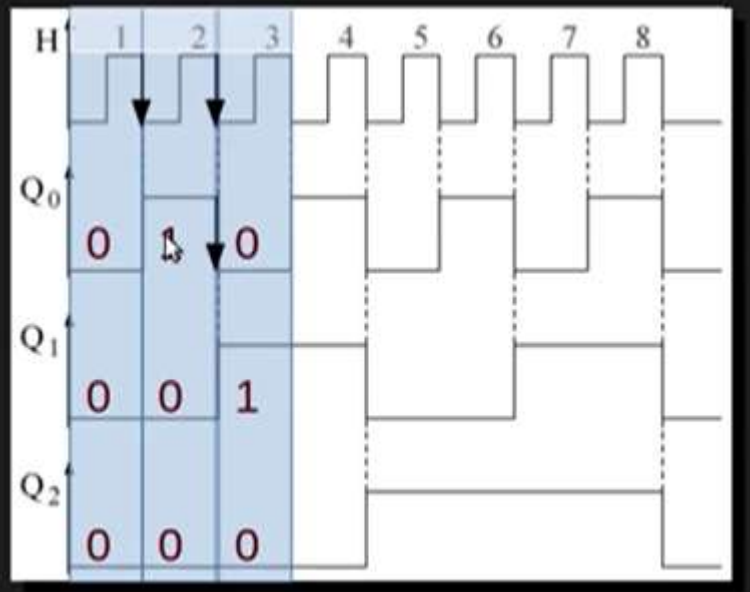
Example of a counter:



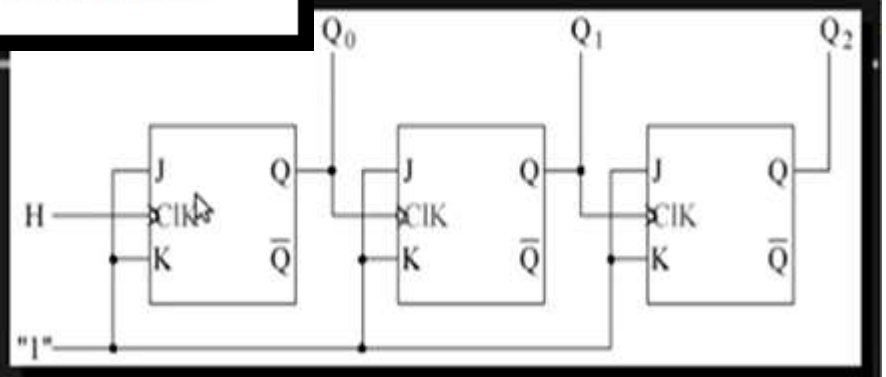


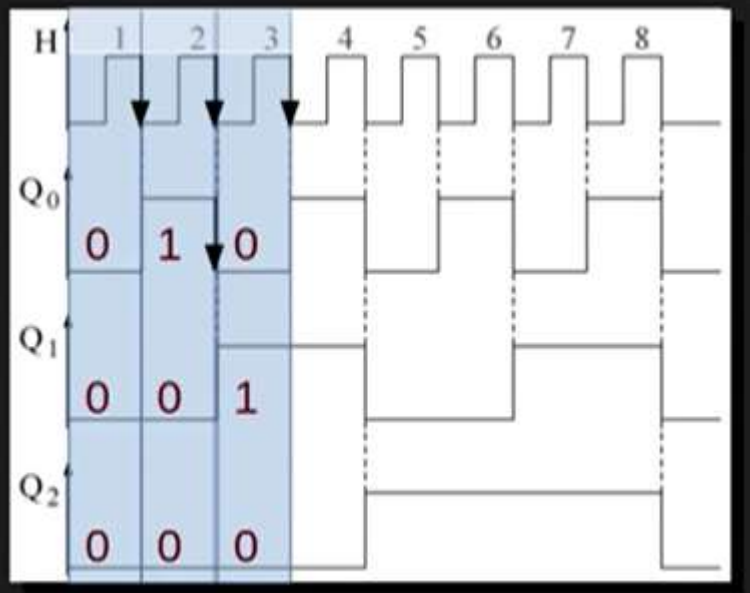
Example of a counter:



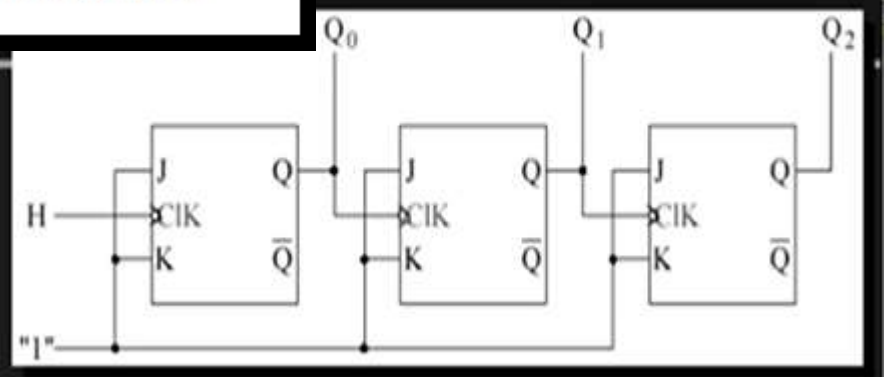


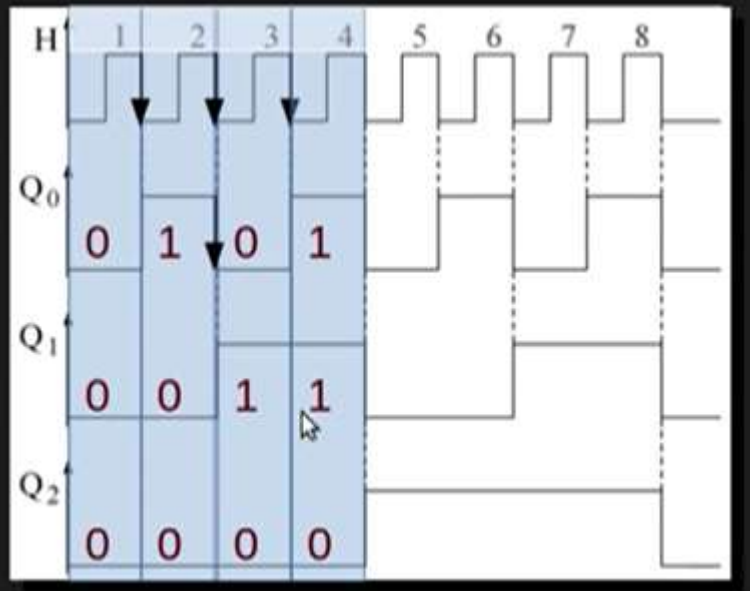
Example of a counter:



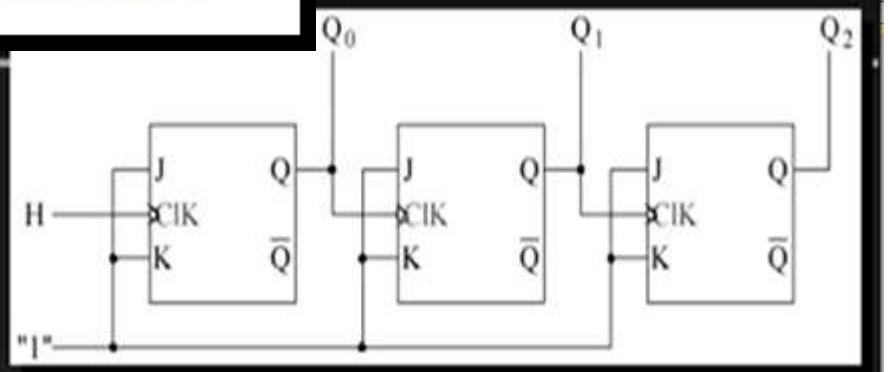


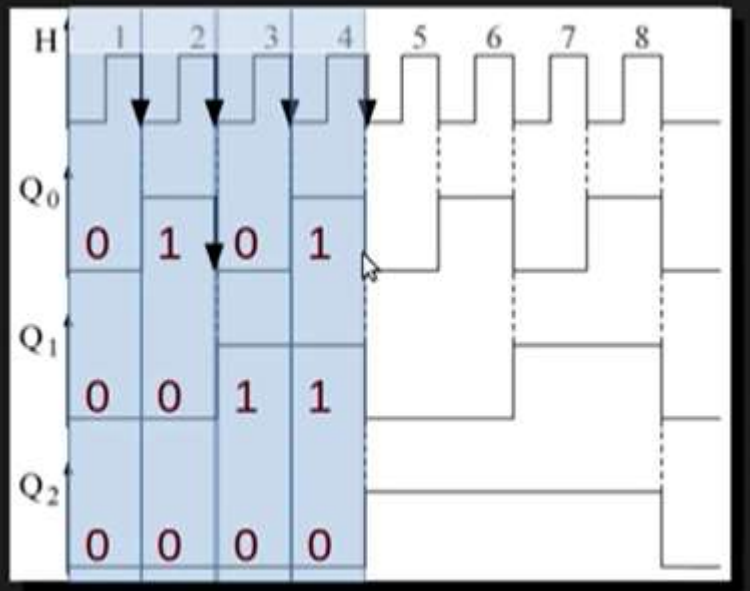
Example of a counter:



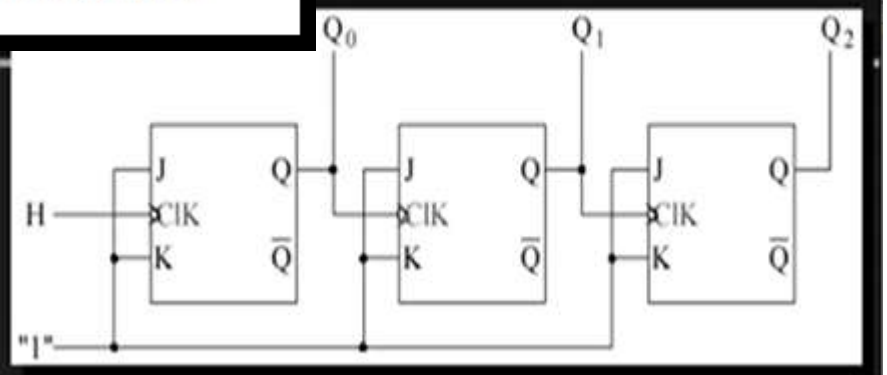


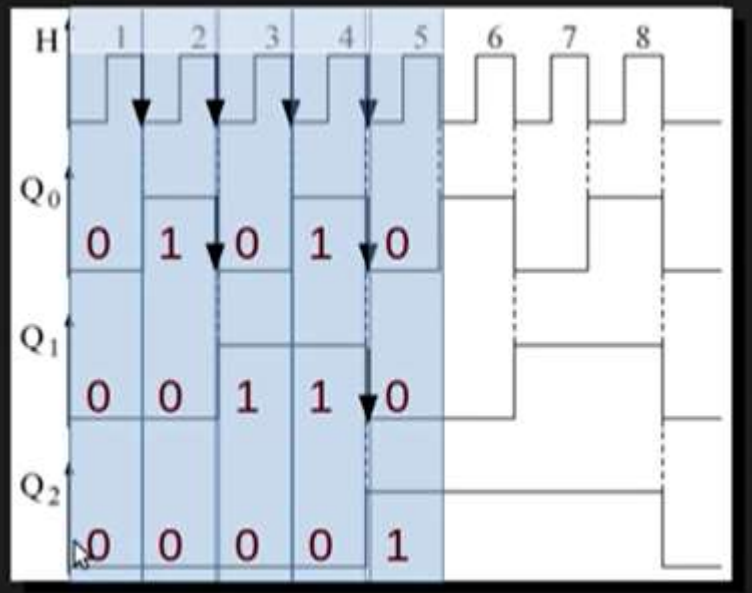
Example of a counter:



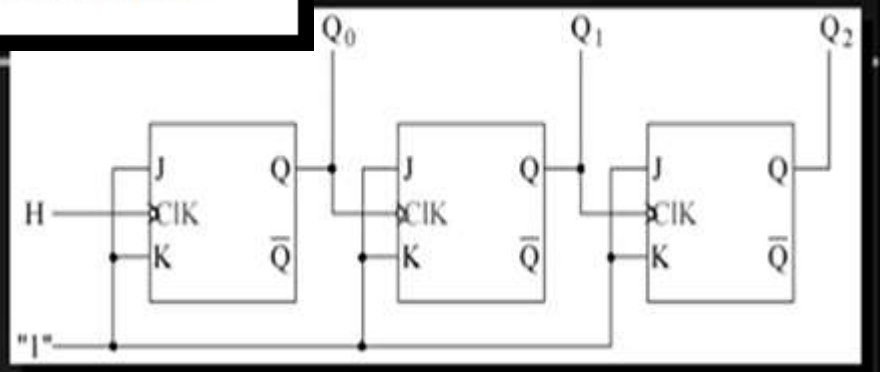


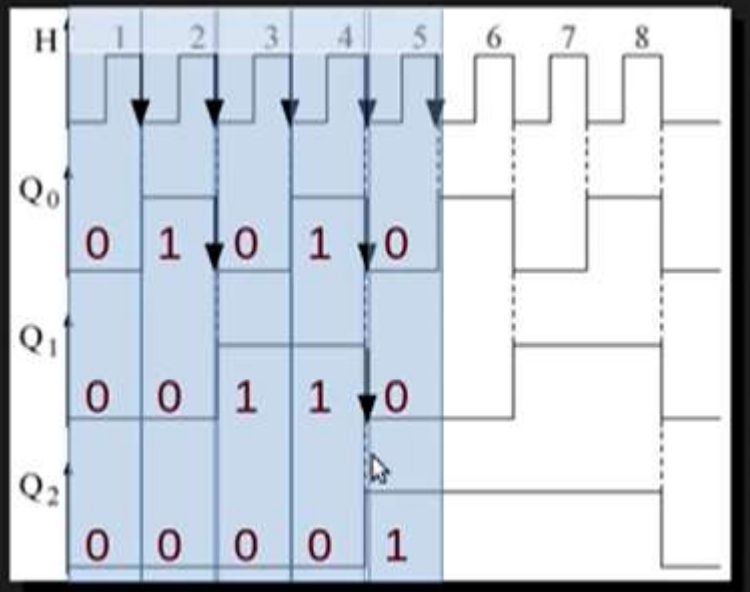
Example of a counter:



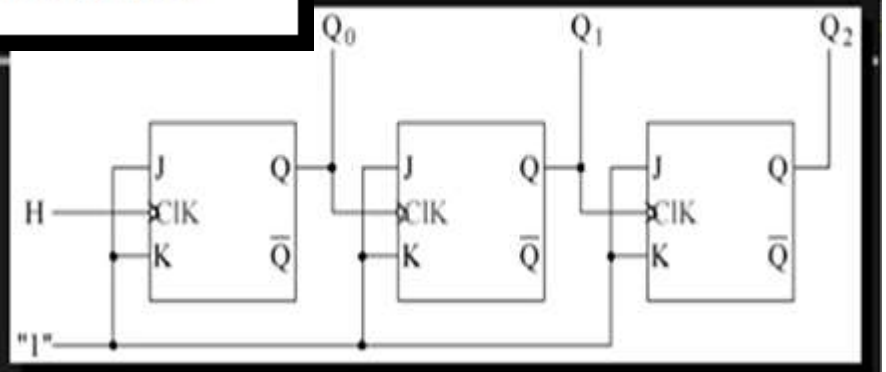


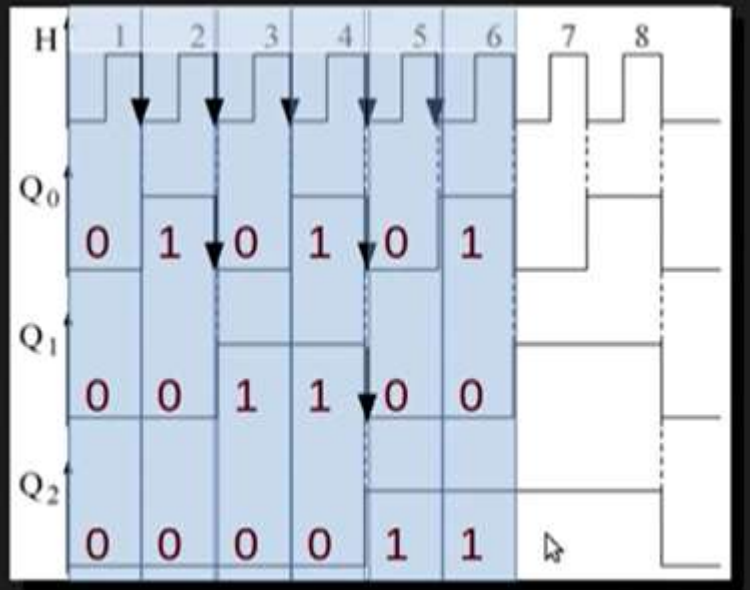
Example of a counter:



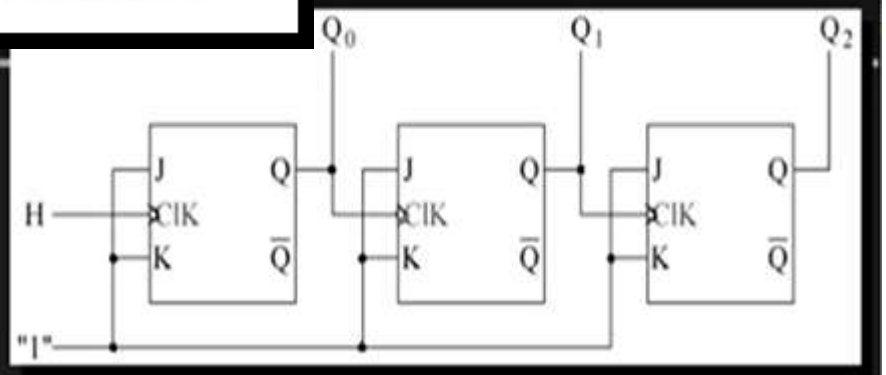


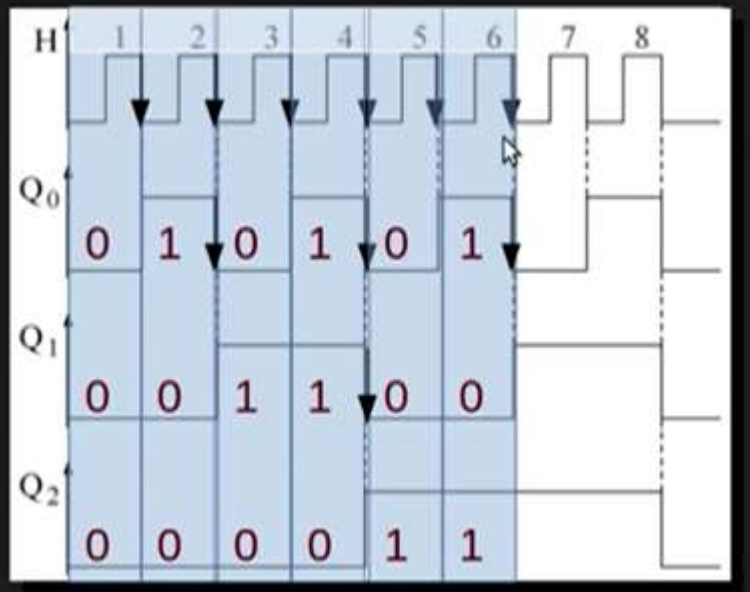
Example of a counter:



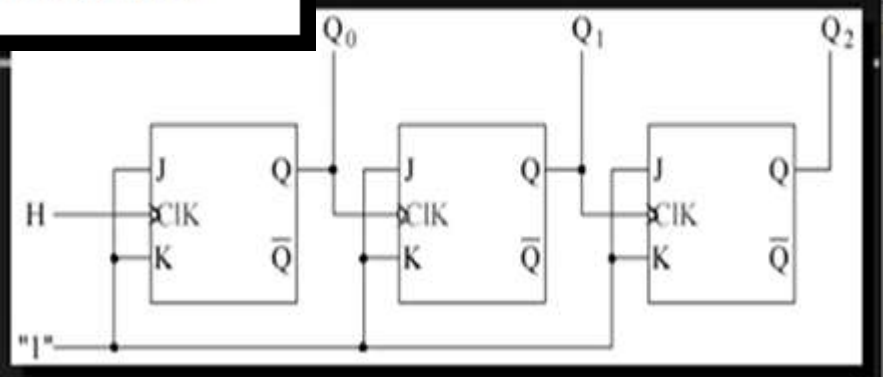


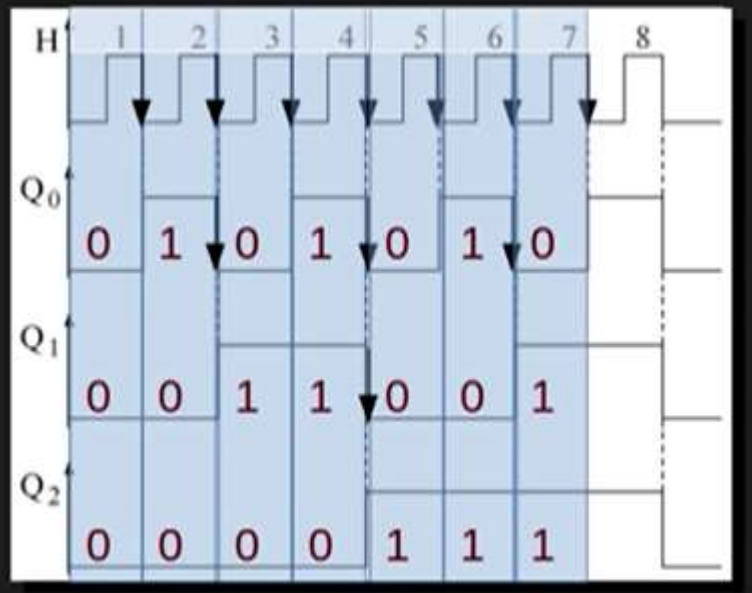
Example of a counter:



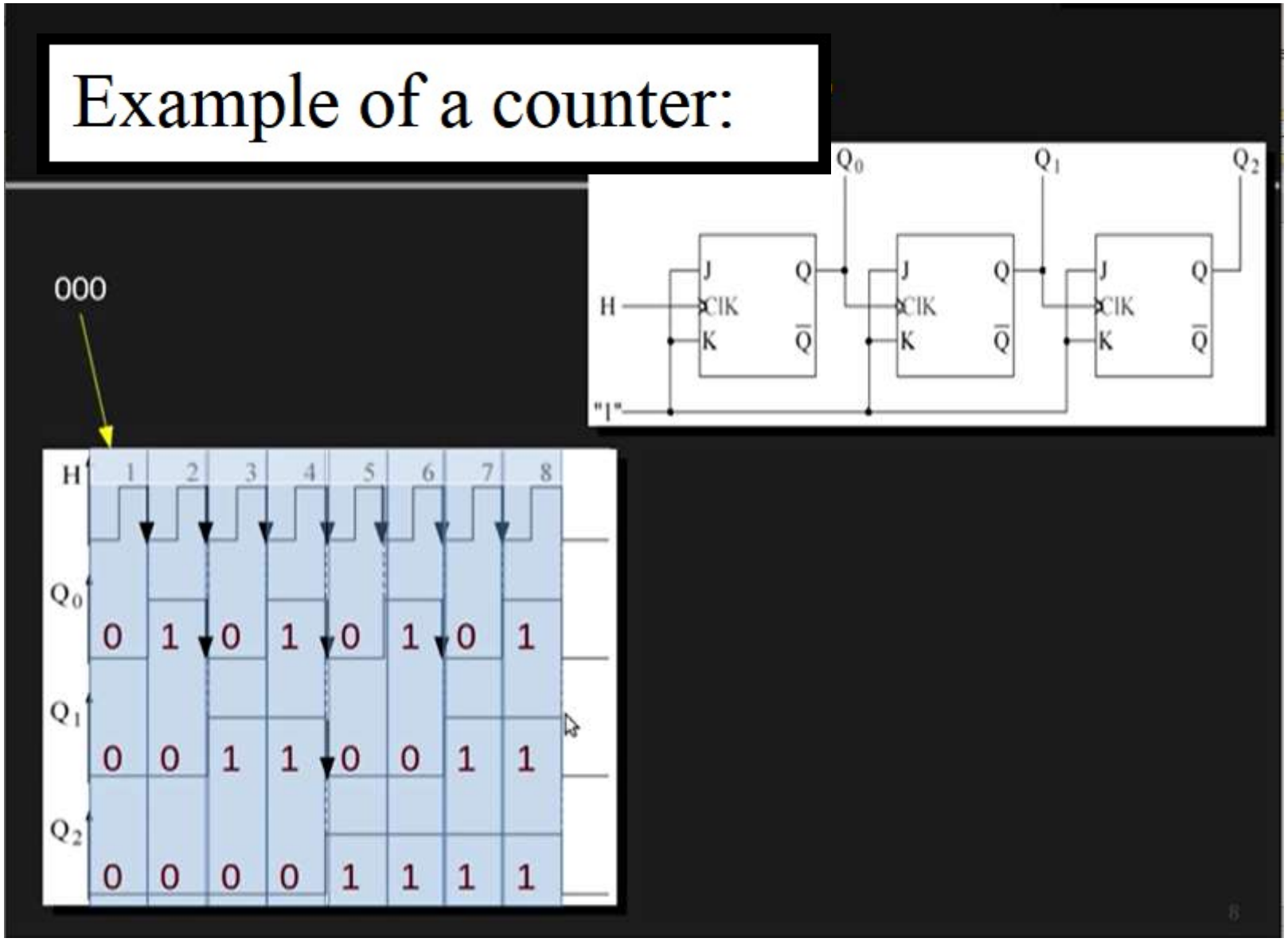


Example of a counter:

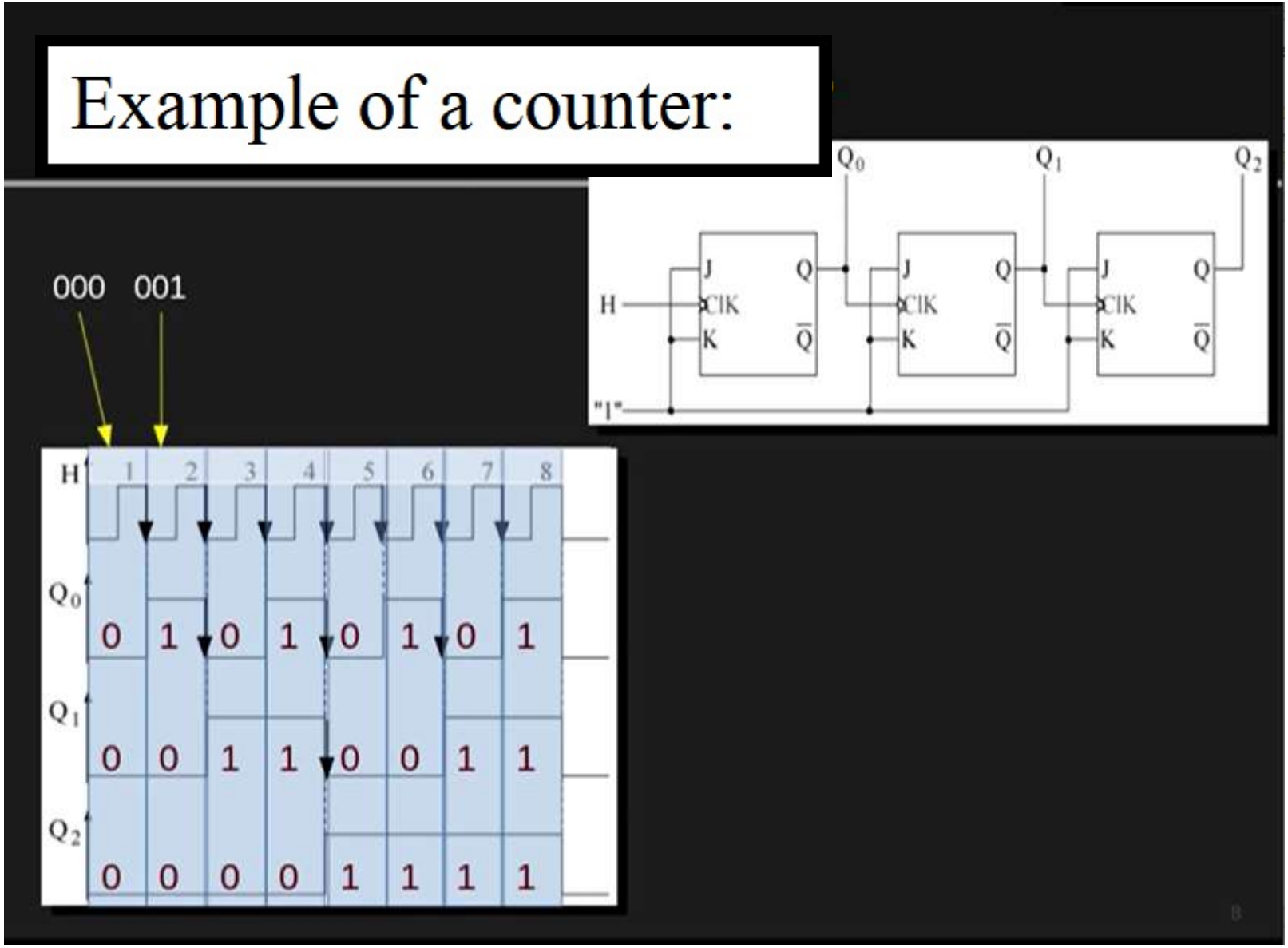




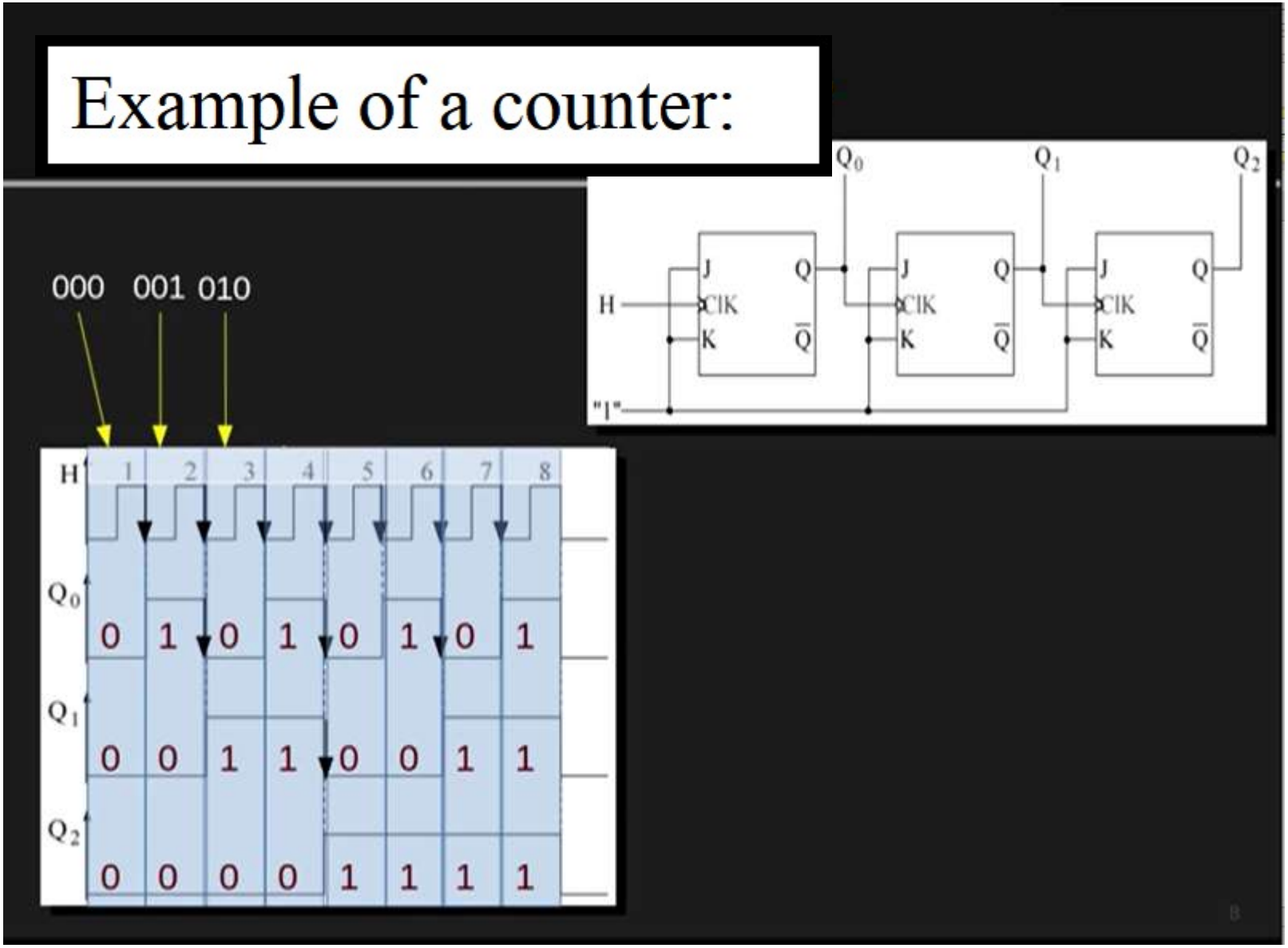
Example of a counter:



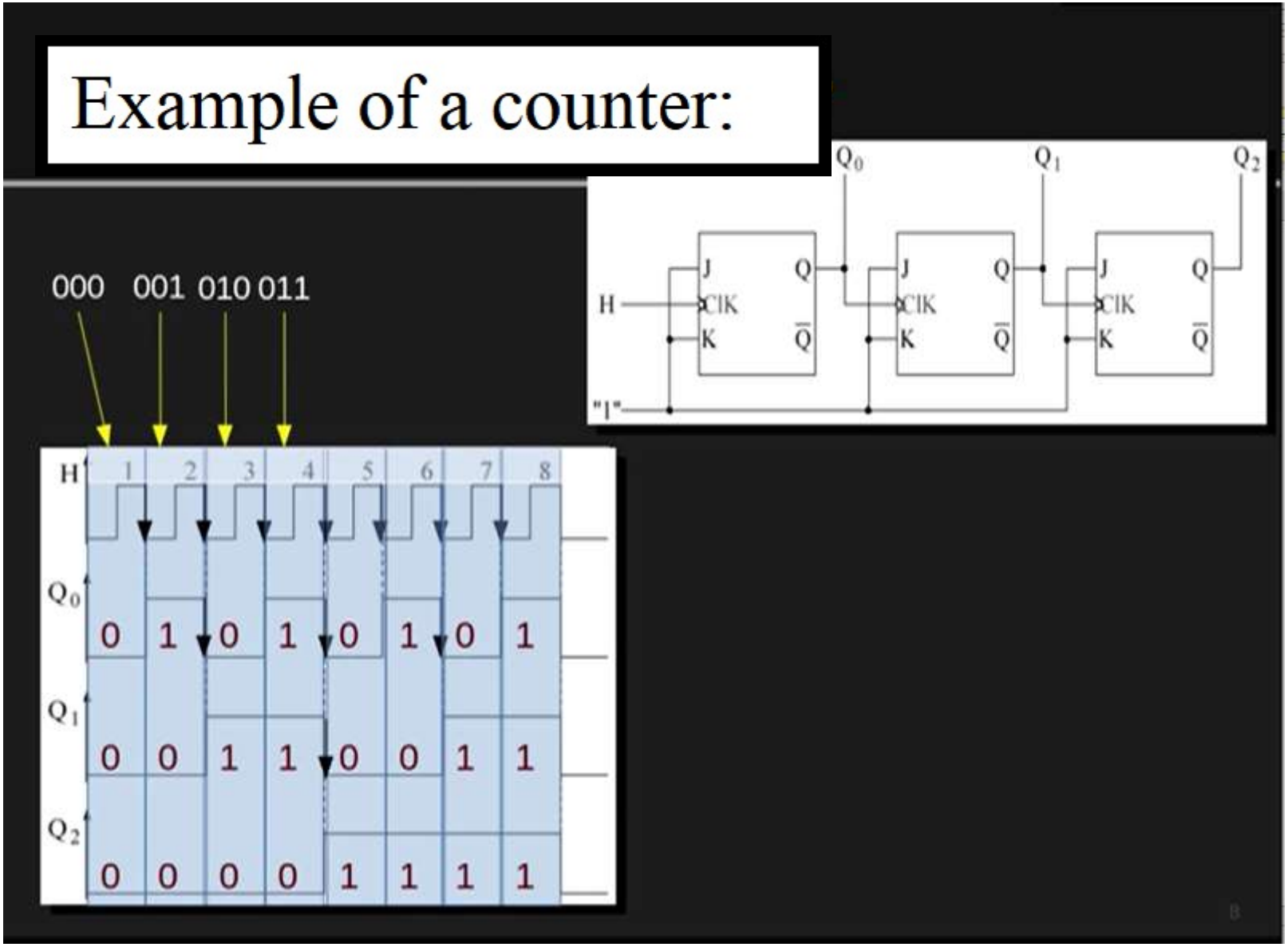
Example of a counter:



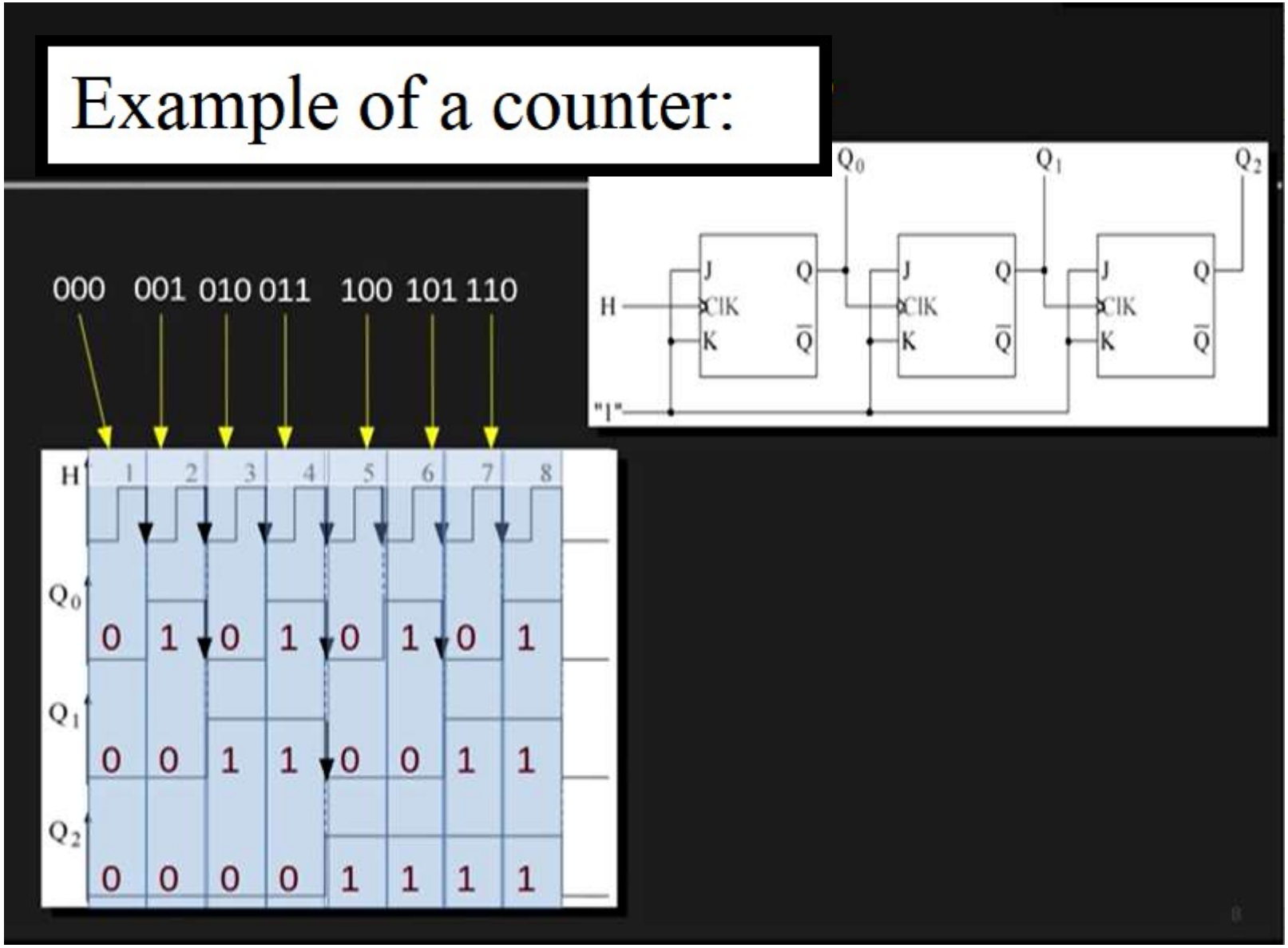
Example of a counter:



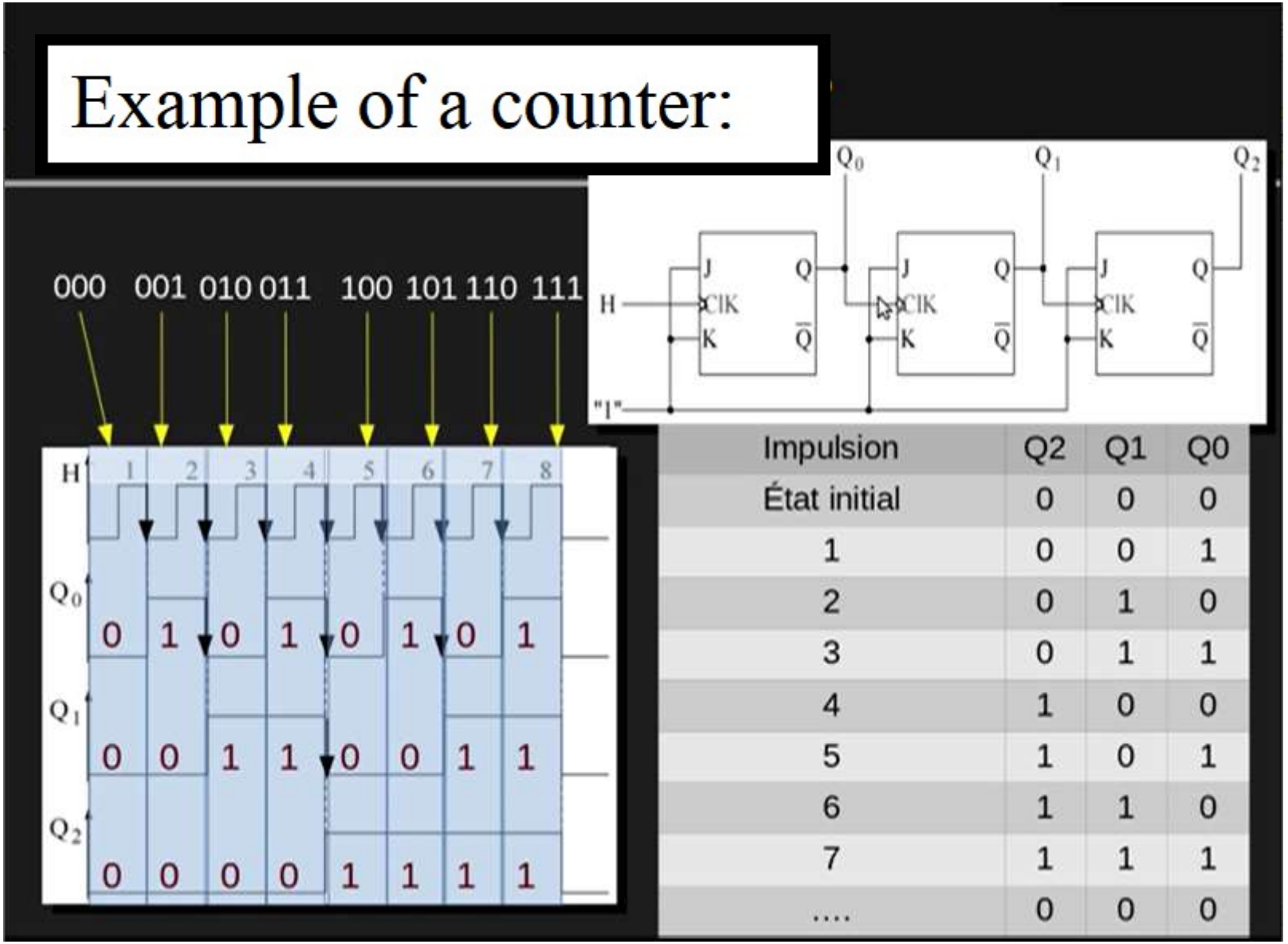
Example of a counter:



Example of a counter:



Example of a counter:



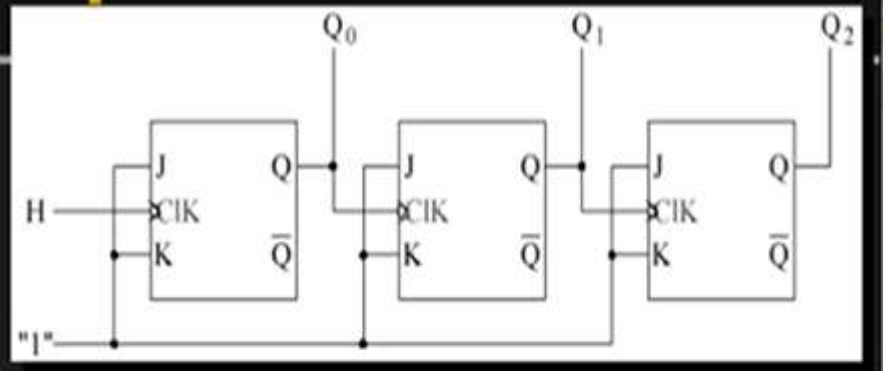
Impulsion	Q2	Q1	Q0
État initial	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
....	0	0	0

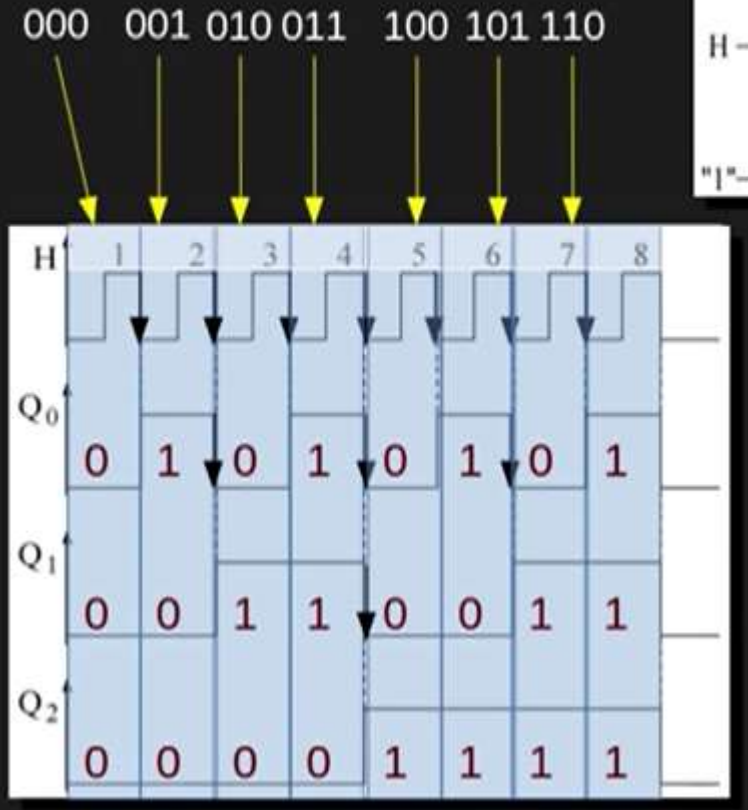
Décompteurs

Décompteurs

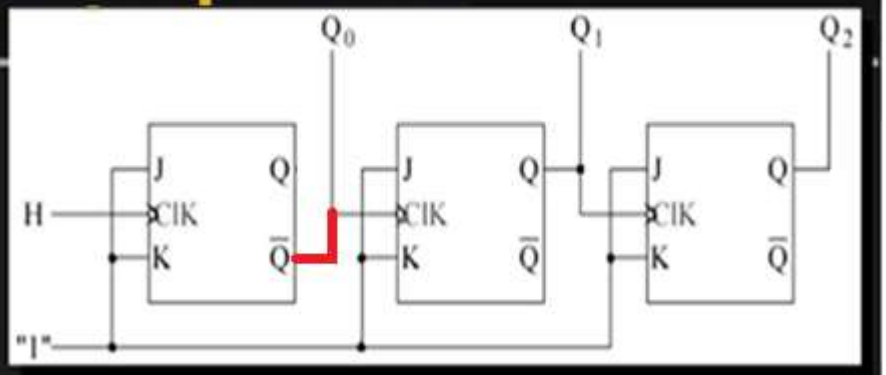
- Il suffit de relier la sortie Q_{barre} de l'étage i à l'entrée CLK de l'étage i+1

Exemple de compteur

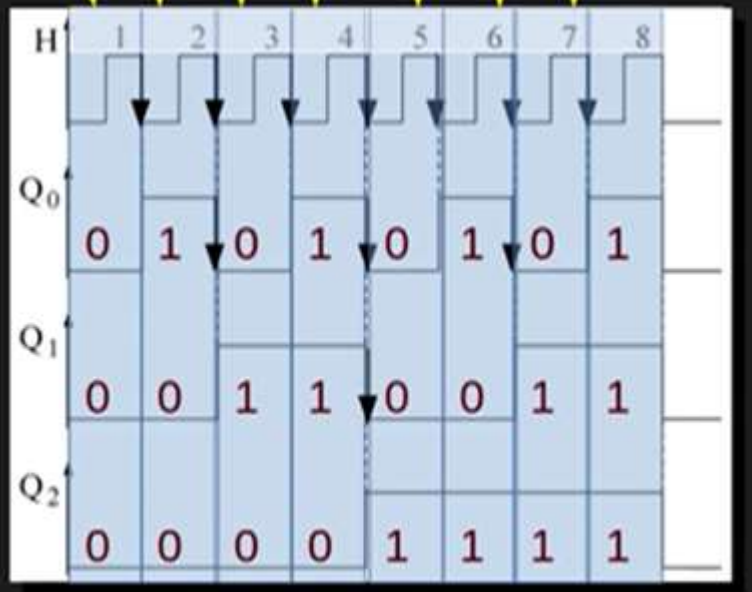




Exemple de Décompteurs

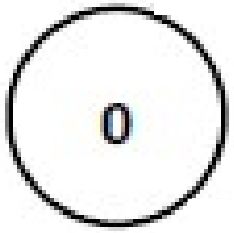


000 001 010 011 100 101 110



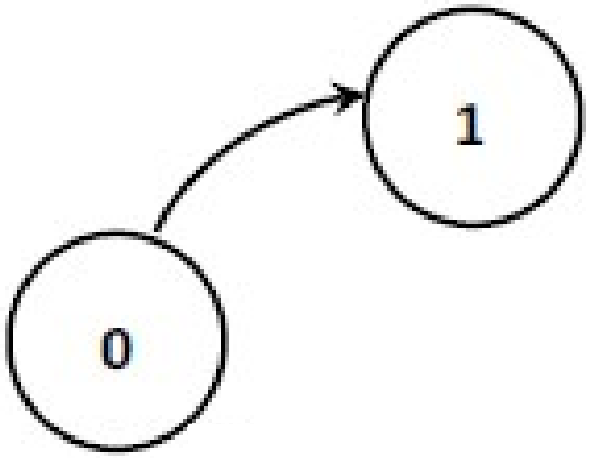
Example of synchronous counter

- Example: We can easily construct the logic diagram of a modulo 5 counter from its following state diagram:



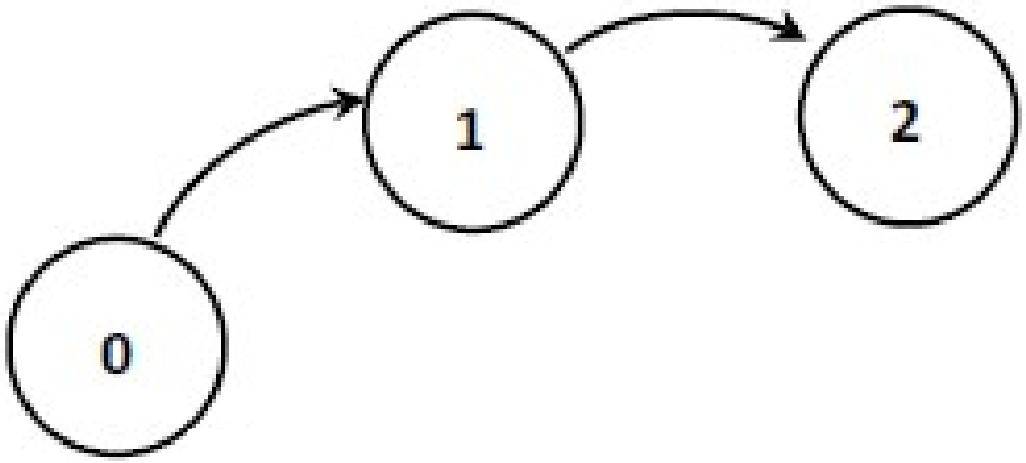
Example of synchronous counter

- Example: We can easily construct the logic diagram of a modulo 5 counter from its following state diagram:



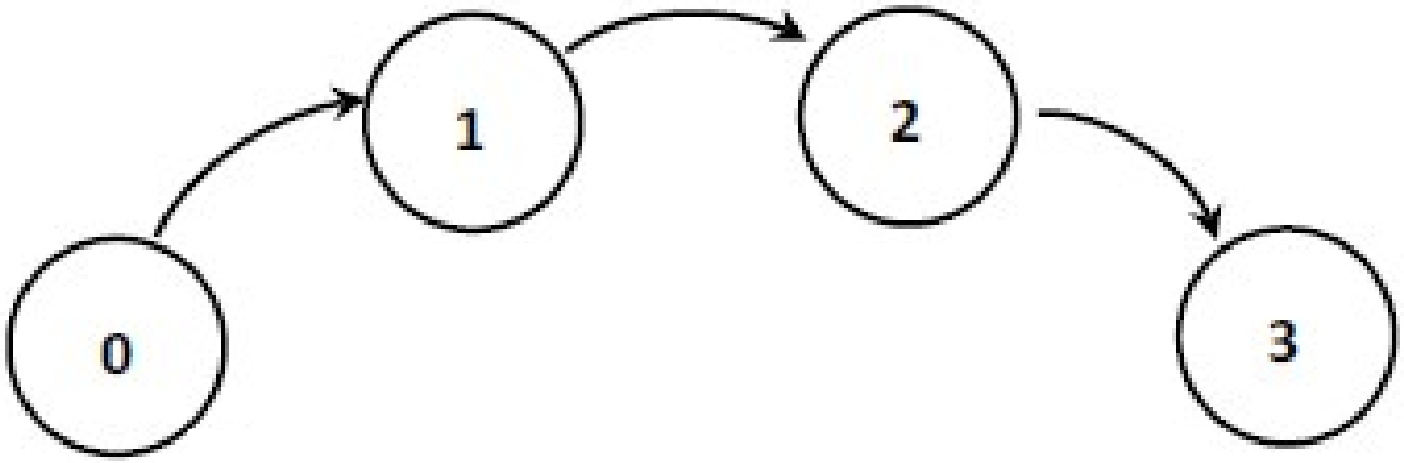
Example of synchronous counter

- Example: We can easily construct the logic diagram of a modulo 5 counter from its following state diagram:



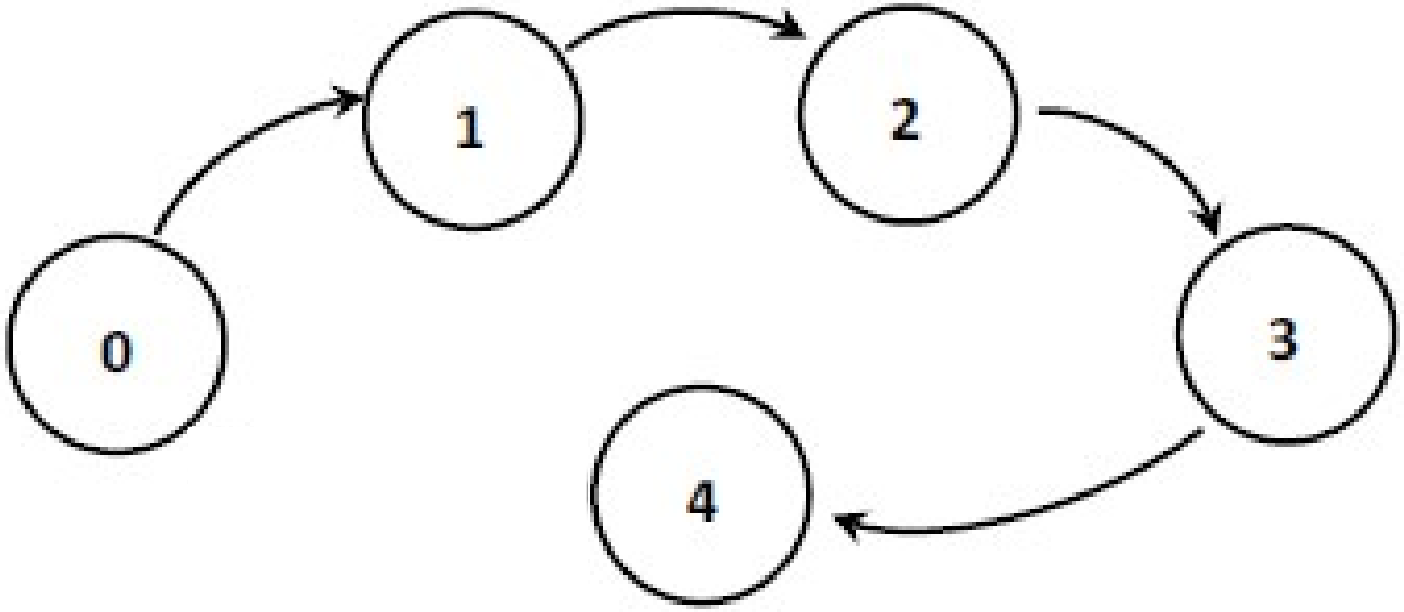
Example of synchronous counter

- Example: We can easily construct the logic diagram of a modulo 5 counter from its following state diagram:



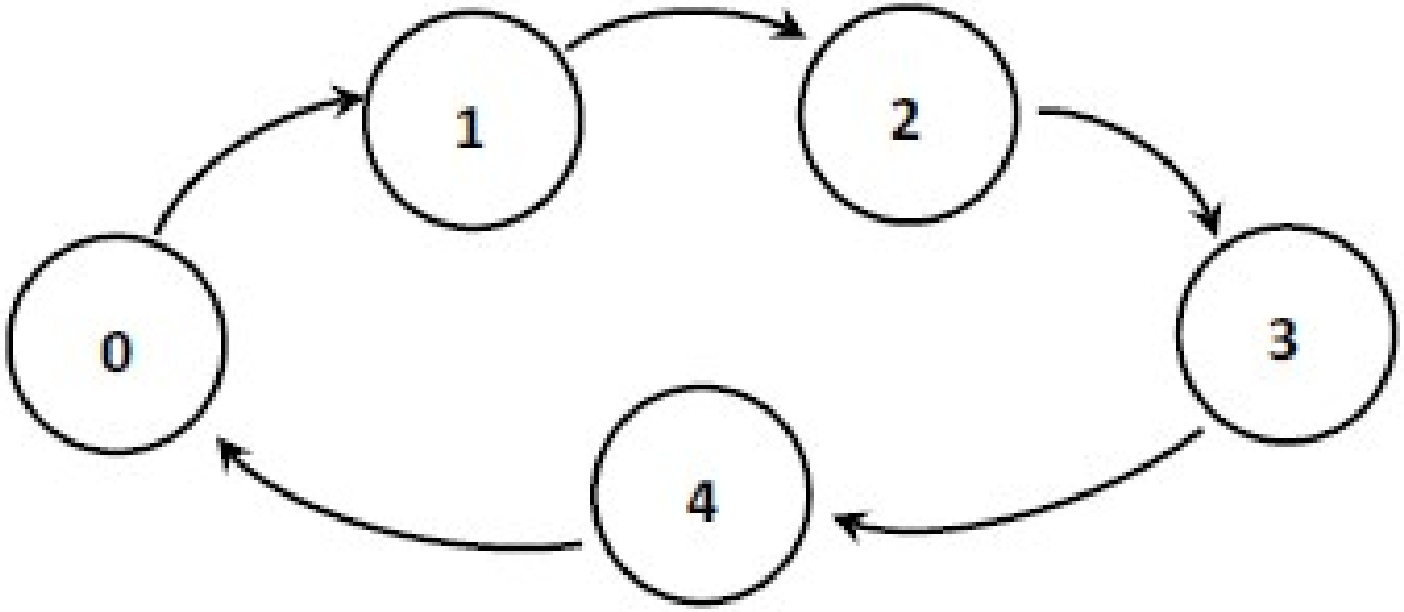
Example of synchronous counter

- Example: We can easily construct the logic diagram of a modulo 5 counter from its following state diagram:



Example of synchronous counter

- Example: We can easily construct the logic diagram of a modulo 5 counter from its following state diagram:



Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state		
q2	q1	q0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state		
q2	q1	q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	0

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state			Flip-flop 2	Flip-flop 1	Flip-flop 0
q2	q1	q0	Q2	Q1	Q0	D2	D1	D0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	0	0	0	0	0	0

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state		
q2	q1	q0

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state		
q2	q1	q0	Q2	Q1	Q0

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state		
q2	q1	q0	Q2	Q1	Q0
0	0	0			

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state		
q2	q1	q0	Q2	Q1	Q0
0	0	0	0	0	1

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state		
q2	q1	q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1			

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state		
q2	q1	q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state		
q2	q1	q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0			

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state		
q2	q1	q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state		
q2	q1	q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1			

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state		
q2	q1	q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state		
q2	q1	q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0			

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state		
q2	q1	q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	0

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state			Flip-flop 2	Flip-flop 1	Flip-flop 0
q2	q1	q0	Q2	Q1	Q0			
0	0	0	0	0	1			
0	0	1	0	1	0			
0	1	0	0	1	1			
0	1	1	1	0	0			
1	0	0	0	0	0			

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state			Flip-flop 2	Flip-flop 1	Flip-flop 0
q2	q1	q0	Q2	Q1	Q0	D2	D1	D0
0	0	0	0	0	1			
0	0	1	0	1	0			
0	1	0	0	1	1			
0	1	1	1	0	0			
1	0	0	0	0	0			

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state			Flip-flop 2	Flip-flop 1	Flip-flop 0
q2	q1	q0	Q2	Q1	Q0	D2	D1	D0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0			
0	1	0	0	1	1			
0	1	1	1	0	0			
1	0	0	0	0	0			

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state			Flip-flop 2	Flip-flop 1	Flip-flop 0
q2	q1	q0	Q2	Q1	Q0	D2	D1	D0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1			
0	1	1	1	0	0			
1	0	0	0	0	0			

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state			Flip-flop 2	Flip-flop 1	Flip-flop 0
q2	q1	q0	Q2	Q1	Q0	D2	D1	D0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0			
1	0	0	0	0	0			

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state			Flip-flop 2	Flip-flop 1	Flip-flop 0
q2	q1	q0	Q2	Q1	Q0	D2	D1	D0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	0	0	0			

Example of synchronous counter

- The transition table corresponding to this counter will be given as follows:

Current state			Future state			Flip-flop 2	Flip-flop 1	Flip-flop 0
q2	q1	q0	Q2	Q1	Q0	D2	D1	D0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	0	0	0	0	0	0

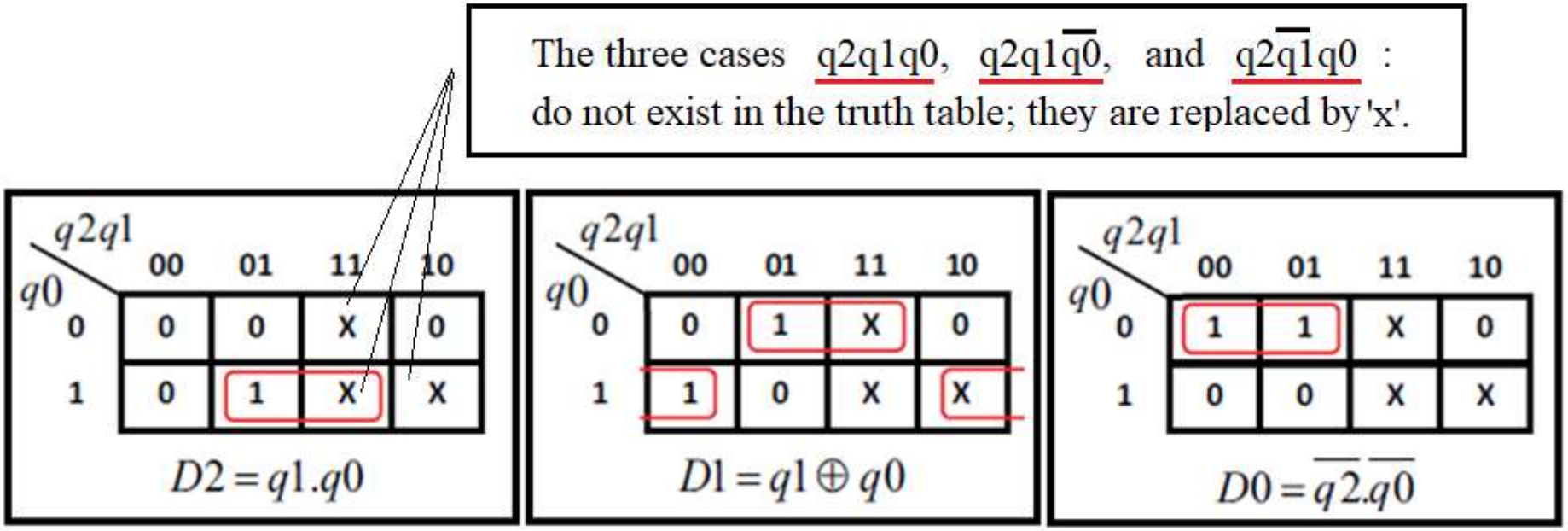
Example of synchronous counter

Current state			Future state			Flip-flop 2	Flip-flop 1	Flip-flop 0
q2	q1	q0	Q2	Q1	Q0	D2	D1	D0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	0	0	0	0	0	0
0	1	0						
0	1	1						
1	0	0						

The three cases $q2q1q0$, $q2q1\overline{q0}$, and $q2\overline{q1}q0$:
do not exist in the truth table; they are replaced by 'x'.

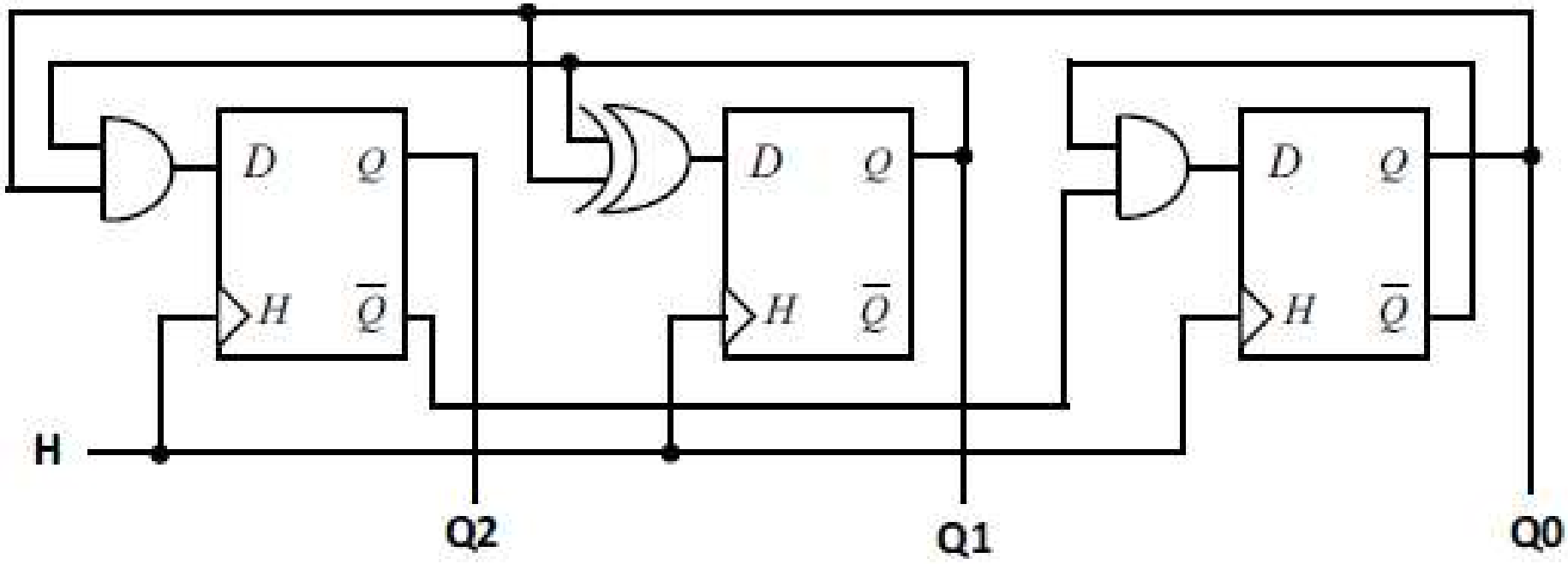
Example of synchronous counter

- The simplified expressions of the flip-flop inputs are provided from the following Karnaugh maps:



Example of synchronous counter

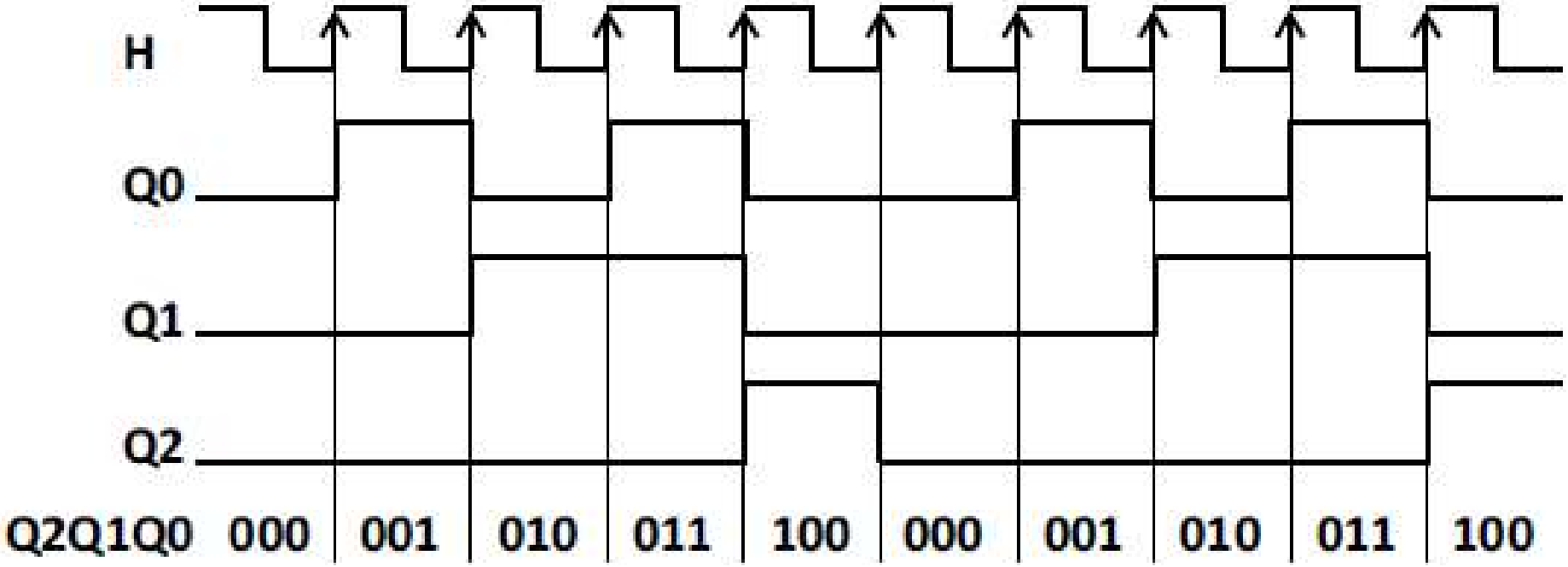
- The logic diagram of this counter will be given as follows:



$D2 = q1.q0$	$D1 = q1 \oplus q0$	$D0 = \overline{q2}.\overline{q0}$

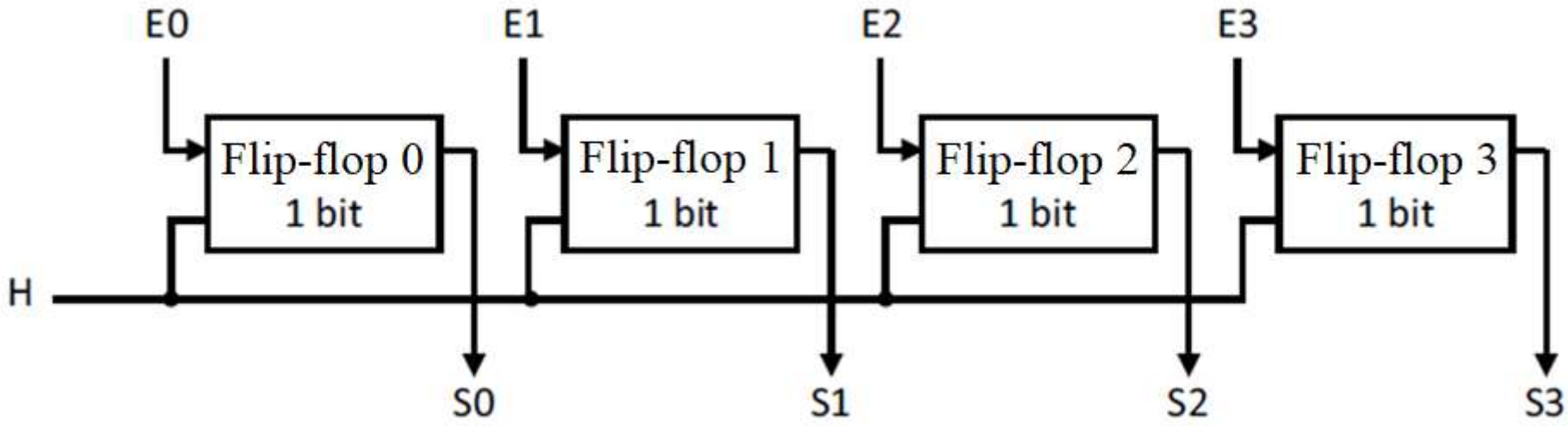
Example of synchronous counter

- Its timing diagram is given as follows:



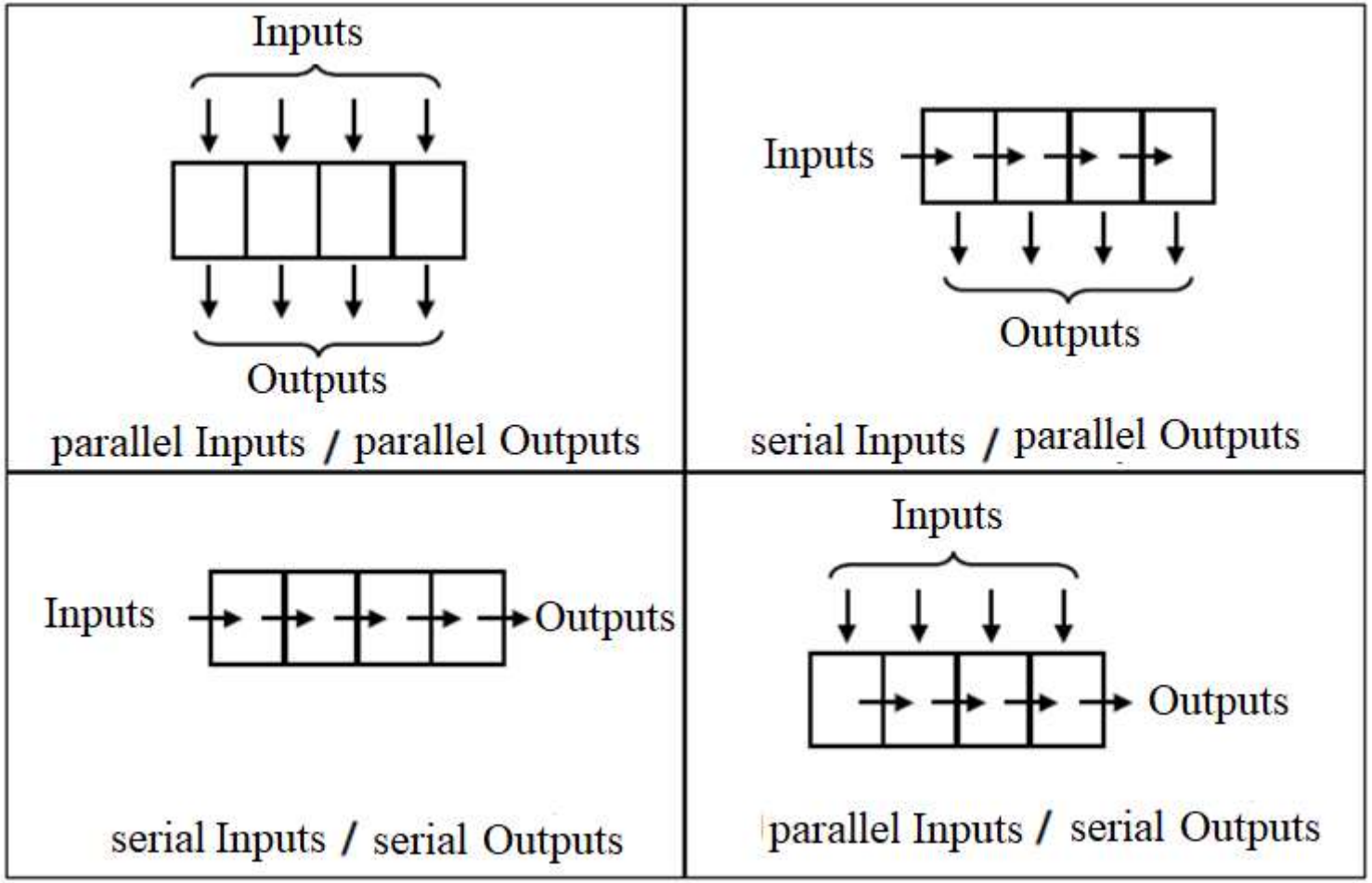
The registers

- A register is a sequential circuit consisting of n flip-flops connected in series to store binary information on n bits.



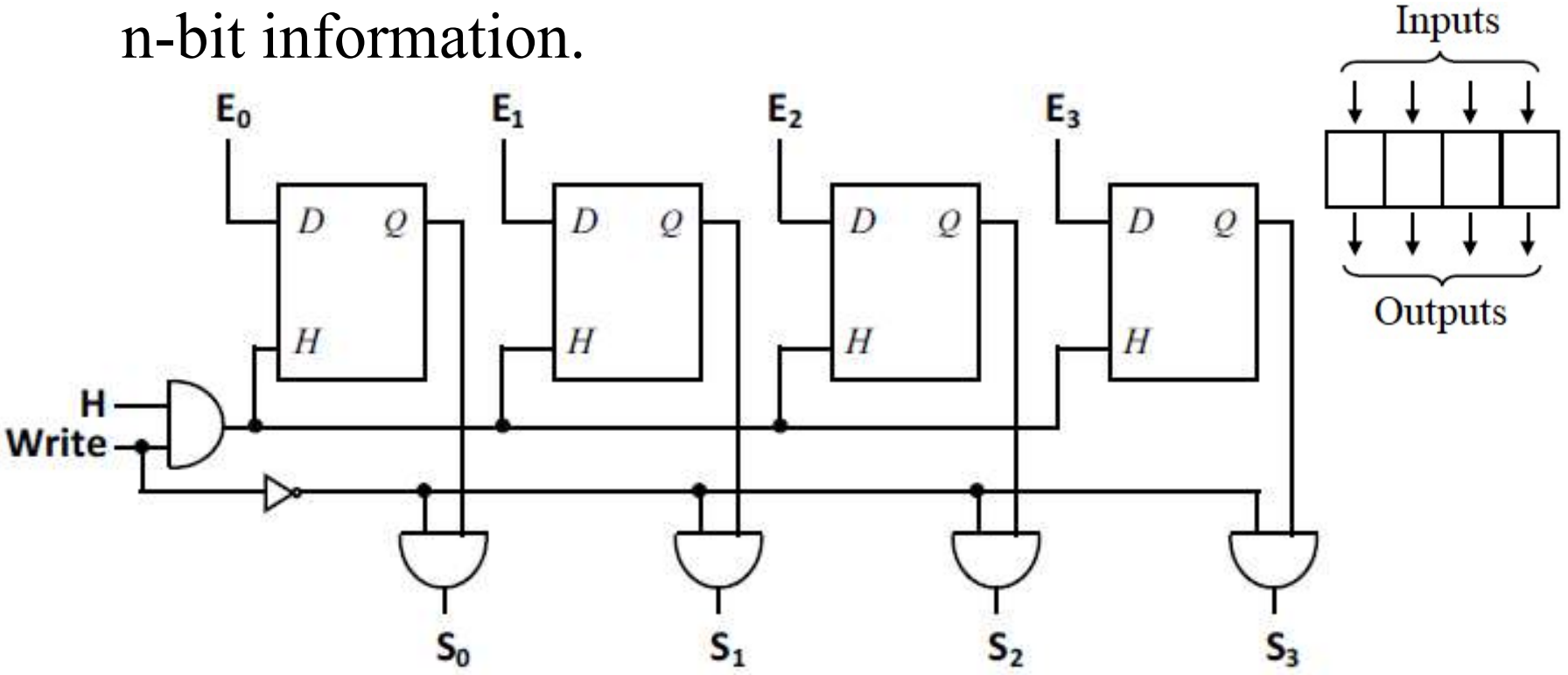
The registers

- Depending on the access mode to the register (read and write), we can distinguish four different types of registers.



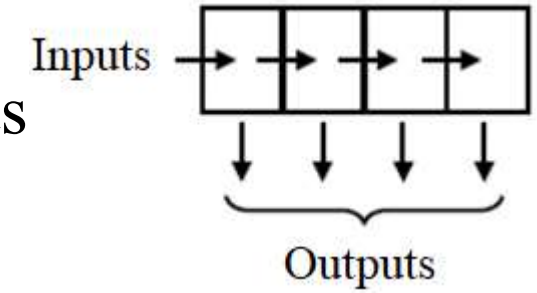
The registers

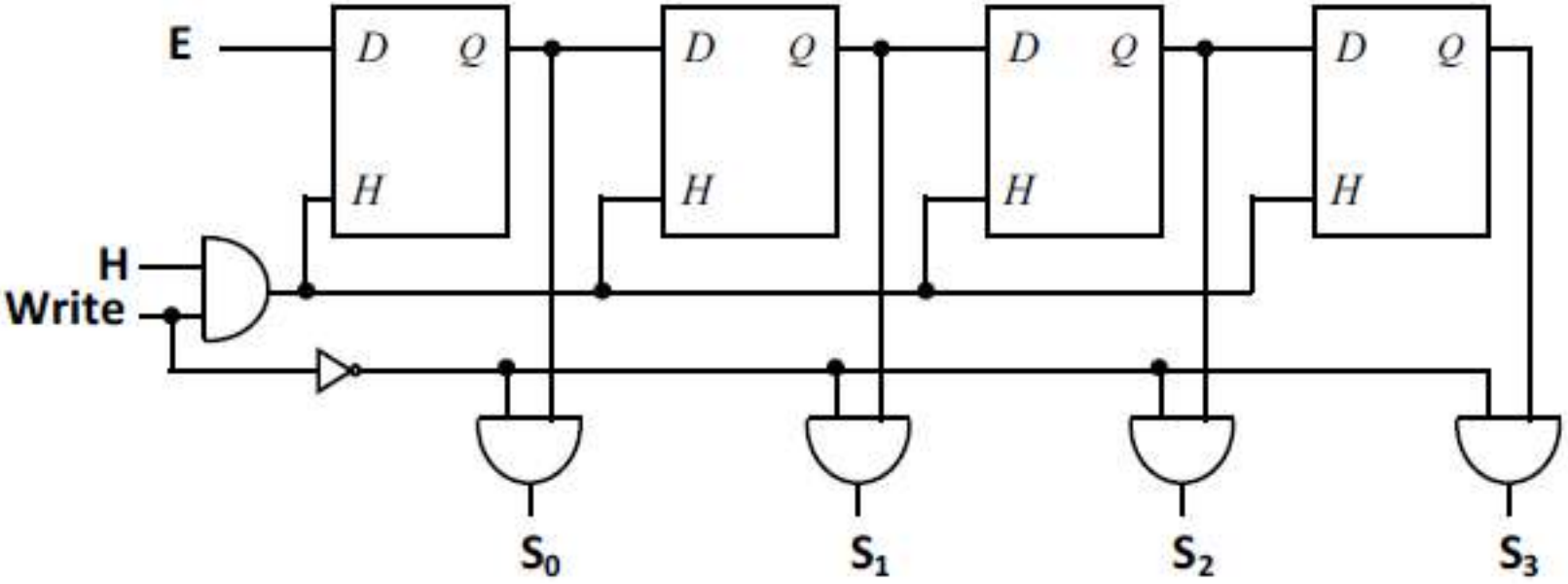
- Parallel input and parallel output registers: these are registers with n data inputs and n data outputs. This type of register is typically used to temporarily store n-bit information.



The registers

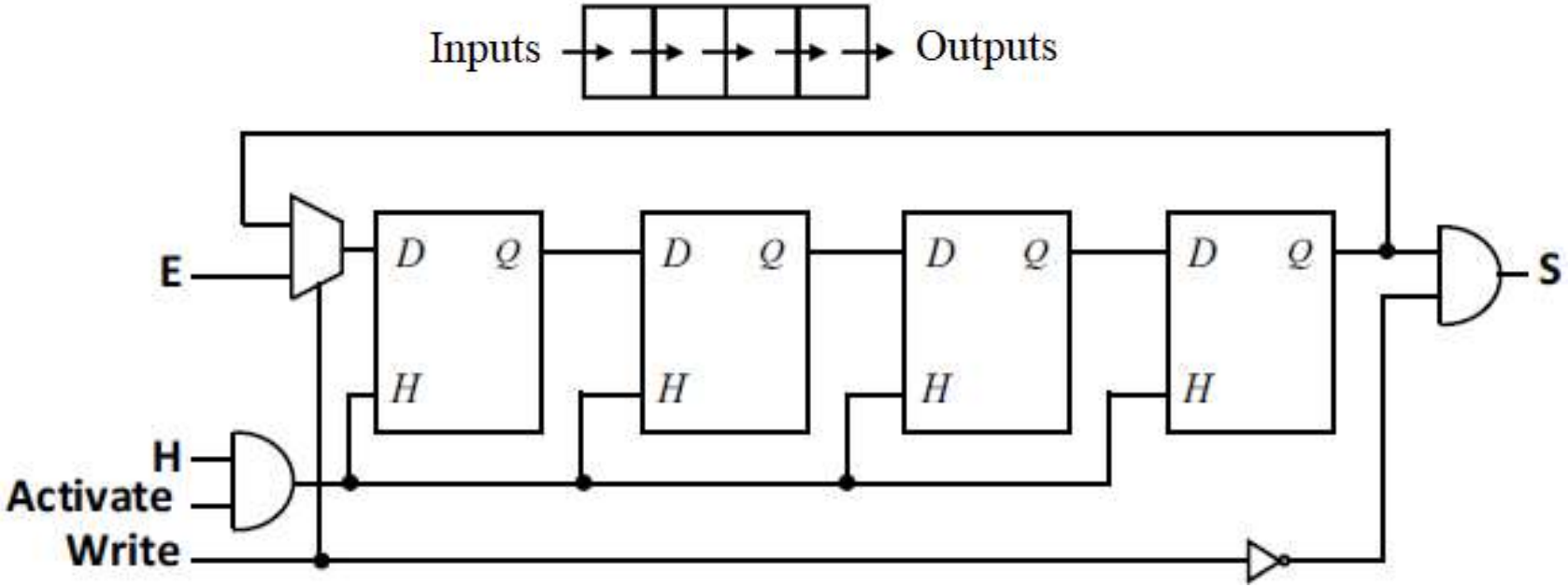
Serial input and parallel output registers: these are registers with a single input and n data outputs.
To write into this type of registers, the bits shifted from one flip-flop to another
the clock rate.





The registers

- Serial input and serial output registers: these are registers with a single input and a single output for data. To read from or write to this type of register, the bits are shifted from one flip-flop to another at the clock rate.



The registers

- Parallel input and serial output registers: these are registers with n inputs and a single output for data. To read from this type of register, the bits are shifted from one flip-flop to another at the clock rate.