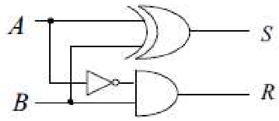
Correcting directed works N°. 02

Exercice : 1. Adder/Subtractor..

1. The circuit that performs subtraction 1 bit by 1 bit (half-subtractor)

A	B	S	R
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

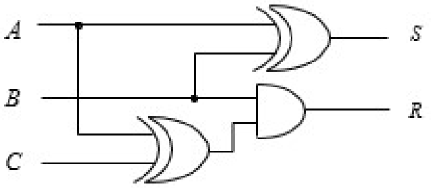
$S = A \oplus B \qquad R = \overline{A}.B$



2. The half-adder/subtractor.

C	A	B	S	R
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	0

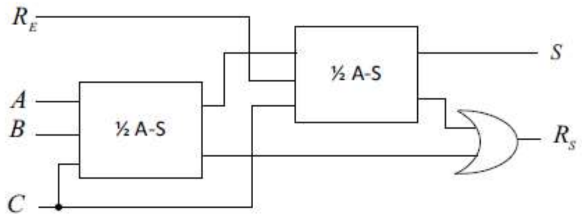
$S = A \oplus B \qquad R = (C \oplus A).\, B$



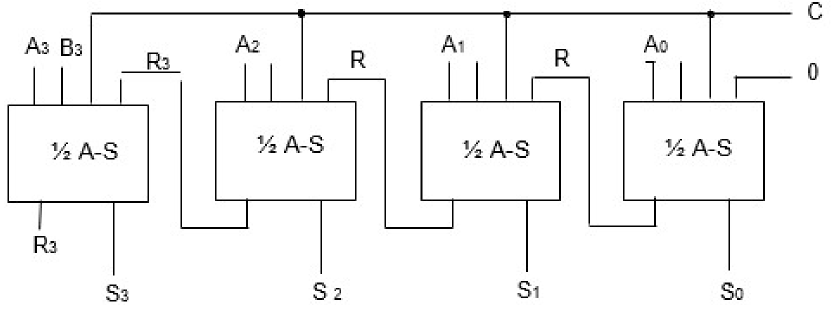
3. The full adder/subtractor 1 bit by 1 bit with input carry.

C	R_E	A	B	S	R
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	1	1
1	0	1	0	1	0
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	0	1
1	1	1	0	0	0
1	1	1	1	1	1

$$S = A \oplus B \oplus R_E$$
$$R = (C \oplus A \oplus B).R_E + (C \oplus A).B$$



4. The logical diagram of a 4-bit by 4-bit adder/subtractor.

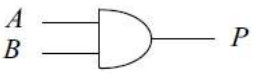


Exercice 2. Multiplier.

1. The circuit that performs 1-bit by 1-bit multiplication.

A	B	P
0	0	0
0	1	0
1	0	0
1	1	1

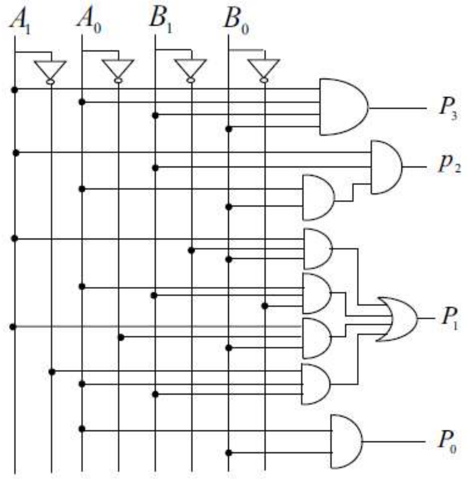
$$P = A.B$$



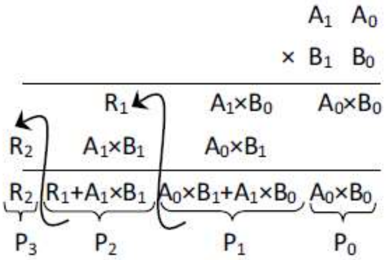
2. The 2-bit by 2-bit multiplier.

A1	A0	B1	B0	P3	P2	P1	P0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

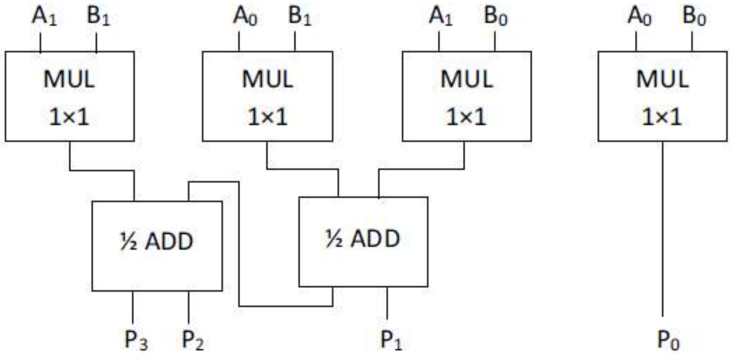
$$P_3 = A_1.\mathrm{A}_0.\mathrm{B}_1.\mathrm{B}_0$$
$$P_2 = A_1.B_1.(\overline{A_0} + \overline{B_0}) = A_1.B_1.\overline{A_0.B_0}$$
$$P_1 = A_1.\overline{B_1}.B_0 + A_0.B_1.\overline{B_0} + A_1.\overline{A_0}.B_0 + \overline{A_1}.A_0.B_1$$
$$P_0 = \mathrm{A}_0.\mathrm{B}_0$$



3. The 2-bit by 2-bit multiplier constructed from 1-bit by 1-bit multipliers of half-adders.



$$P_3 = R_2$$
$$P_2 = R_1 + A_1 \times B_1$$
$$P_1 = A_0 \times B_1 + A_1 \times B_0$$
$$P_0 = \mathrm{A}_0.\mathrm{B}_0$$



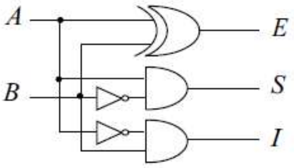
Exercise 3. Comparator

1. The circuit that performs 1-bit by 1-bit comparison

A	B	E	S	I
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

$$E = \overline{A}.\overline{B} + A.B = \overline{A \oplus B}$$

$$S = A.\overline{B} \qquad I = \overline{A}.B$$

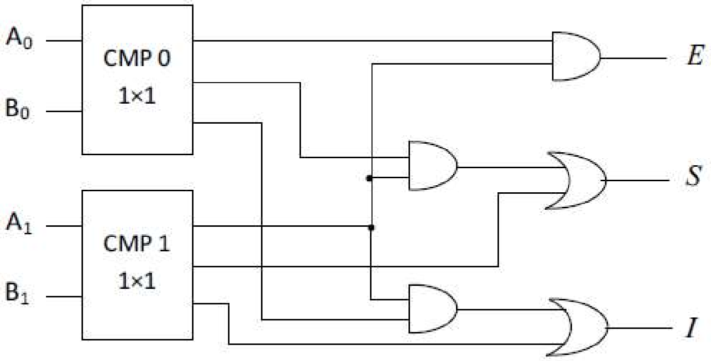


2. The 2-bit comparator using 1-bit comparators and logical gates.7

$$E = 1 \Rightarrow A = B \Rightarrow (A_1 = B_1) et (A_0 = B_0) \Rightarrow E = E_1 E_0$$

$$S = 1 \Rightarrow A > B \Rightarrow (A_1 > B_1) ou[(A_1 = B_1) et (A_0 > B_0)] \Rightarrow S = S_1 + E_1 S_0$$

$$I = 1 \Rightarrow A < B \Rightarrow (A_1 < B_1) ou[(A_1 = B_1) et (A_0 < B_0)] \Rightarrow S = I_1 + E_1 I_0$$

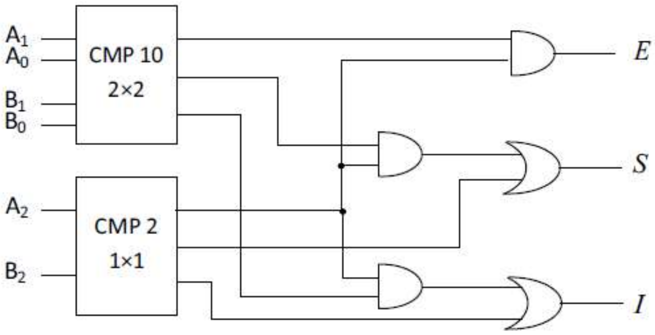


3. The logical diagram of a 3-bit comparator.

$$E = 1 \Rightarrow A = B \Rightarrow (A_2 = B_2) et (A_1 A_0 = B_1 B_0) \Rightarrow E = E_2 E_{10}$$

$$S = 1 \Rightarrow A > B \Rightarrow (A_2 > B_2) ou[(A_2 = B_2) et (A_1 A_0 > B_1 B_0)] \Rightarrow S = S_2 + E_2 S_{10}$$

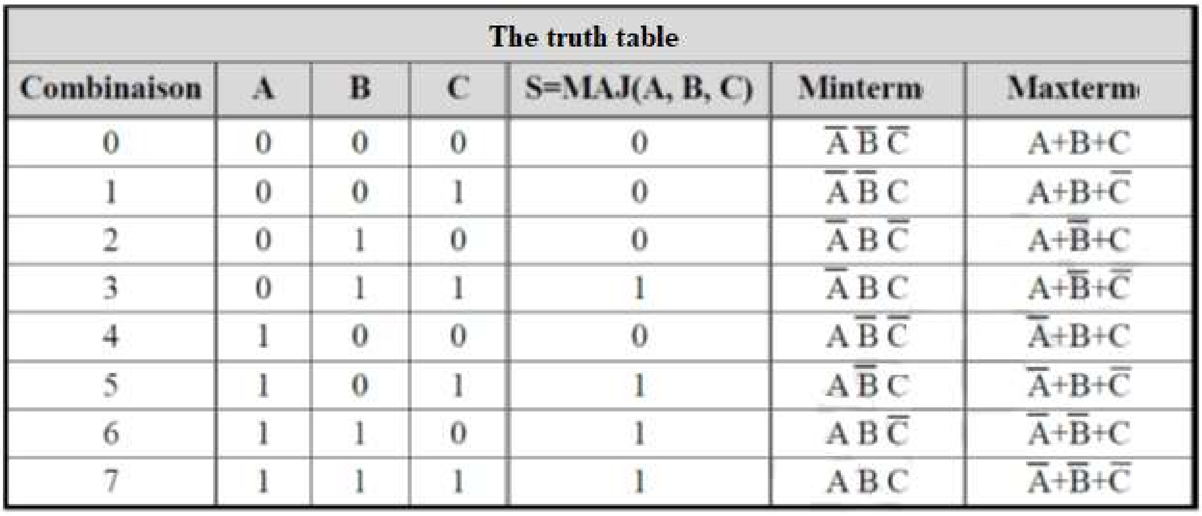
$$I = 1 \Rightarrow A < B \Rightarrow (A_2 < B_2) ou[(A_2 = B_2) et (A_1 A_0 < B_1 B_0)] \Rightarrow S = I_2 + E_2 I_{10}$$



Exercise04 :

1. We notice that MAJ (A, B, C) = 1 for combinations 3, 5, 6, 7. We write the function specified in what is called numeric form:

MAJ= ∑(3,5,6,7), Union of states 3, 5, 6, 7.



The truth table						
Combinaison	A	B	C	S=MAJ(A, B, C)	Minterm	Maxterm
0	0	0	0	0	$\overline{A}\,\overline{B}\,\overline{C}$	A+B+C
1	0	0	1	0	$\overline{A}\,\overline{B}\,C$	A+B+$\overline{C}$
2	0	1	0	0	$\overline{A}\,B\,\overline{C}$	A+$\overline{B}$+C
3	0	1	1	1	$\overline{A}\,B\,C$	A+$\overline{B}$+$\overline{C}$
4	1	0	0	0	$A\,\overline{B}\,\overline{C}$	$\overline{A}$+B+C
5	1	0	1	1	$A\,\overline{B}\,C$	$\overline{A}$+B+$\overline{C}$
6	1	1	0	1	$A\,B\,\overline{C}$	$\overline{A}$+$\overline{B}$+C
7	1	1	1	1	$A\,B\,C$	$\overline{A}$+$\overline{B}$+$\overline{C}$

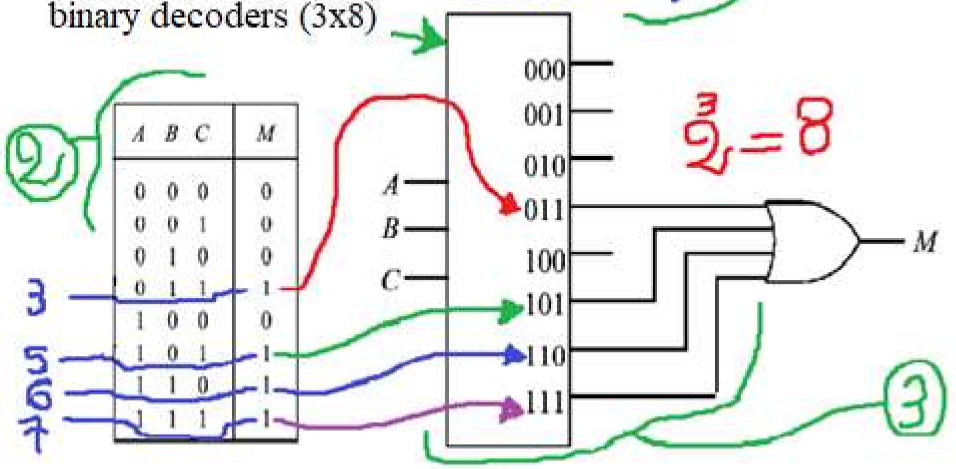
- Function majority M using a decoder and logic gates

$$M = CB\overline{A} + C\overline{B}A + \overline{C}BA + CBA$$

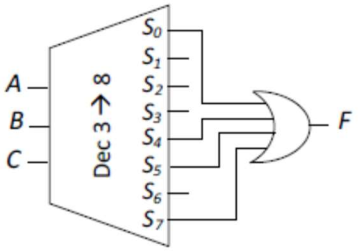
$$= \sum(3,5,6,7)$$

1

binary decoders (3x8)

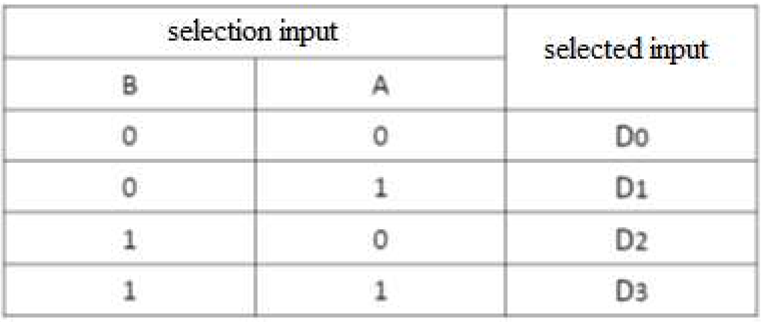


$F(A,B,C)=\sum(0,4,5,7)$



Exercise 5 :

The multiplexer has two control inputs A and B to select one of the four inputs D0, D1, D2, or D3. The selected input carries an index corresponding to the combination of the control inputs. This is translated in the following table

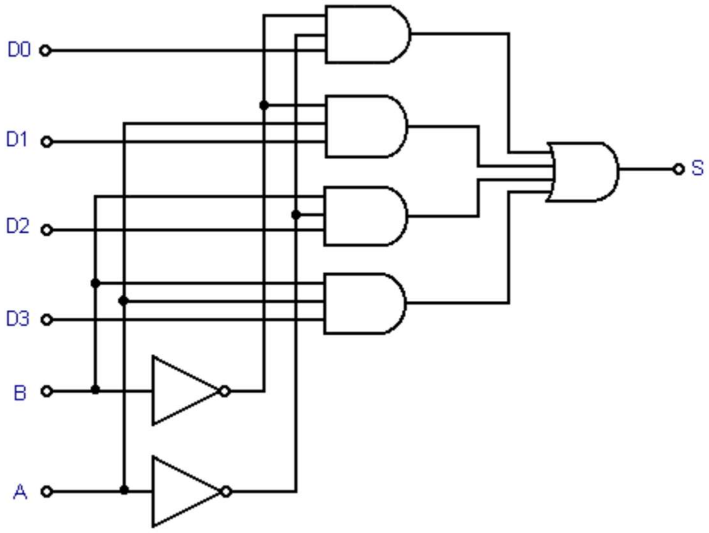


selection input		selected input
B	A	
0	0	D0
0	1	D1
1	0	D2
1	1	D3

The equation for the output S can thus be written as follows:

$$\overline{B}.\overline{A}\ .D0 + \overline{B}.\ A.D1 + B.\ \bar{A}.D2 + B.A.D3$$

Consider the following logic diagram:

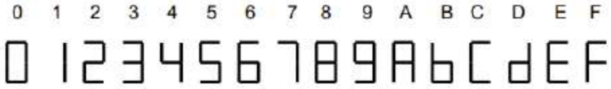


Additional exercises:

Exercise 6 :

1.

7-segment display. The circuit for displaying hexadecimal digits.



X	Y	Z	W	A	B	C	D	E	F	G
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	0	1	1	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

$$A = \overline{X}.Z + Y.Z + X.\overline{W} + X.\overline{Y}.\overline{Z} + \overline{X}.Y.W + \overline{Y}.\overline{W}$$

$$B = \overline{X}.\overline{Y} + \overline{Y}.\overline{W} + \overline{X}.\overline{Z}.\overline{W} + \overline{X}.Z.W + X.\overline{Z}.W$$

$$C = \overline{X}.\overline{Z} + \overline{X}.W + \overline{X}.Y + X.\overline{Y} + \overline{Z}.W$$

$$D = X.\overline{Z} + \overline{Y}.Z.\overline{W} + \overline{X}.\overline{Y}.\overline{W} + \overline{Y}.Z.W + Y.\overline{Z}.W$$

$$E = Z.\overline{W} + X.Y + X.Z + \overline{Y}.\overline{W}$$

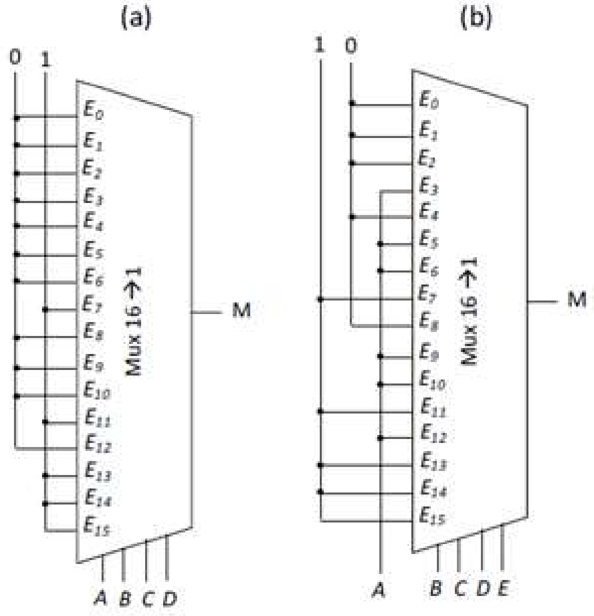
$$F = \overline{Z}.\overline{W} + \overline{X}.Y.\overline{Z} + Y.\overline{W} + X.Z + X.\overline{Y}$$

$$G = \overline{X}.Y.\overline{Z} + \overline{Y}.Z + Z.\overline{W} + X.W + X.\overline{Y}$$

2. Logical functions with multiplexers.

1. The majority function of 4 and 5 variables using a multiplexer (16x1)

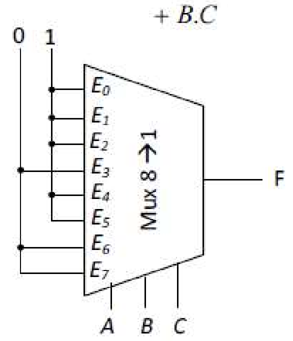
A	B	C	D	M
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1


(a)
0 1
E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15
Mux 16 →1
M
A B C D
(b)
1 0
E0 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15
Mux 16 →1
M
A
B C D E

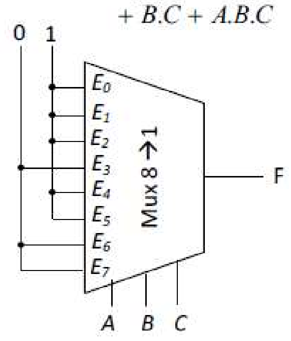
For the 5-variable multiplexer, the majority function occurs when, if we consider the function with only 4 variables where the number of 0s equals the number of 1s, the fifth variable makes the difference. That's why we take the latter and put it in the selection.

2. Implementation of the following functions using an 8x1 multiplexer.

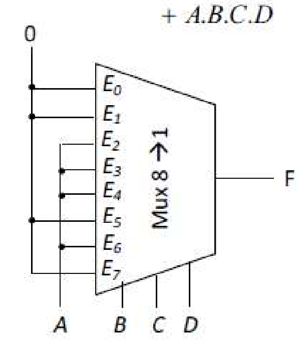
$F(A,B,C) = A.\overline{B} + \overline{A}.\overline{C} + \overline{B}.C$



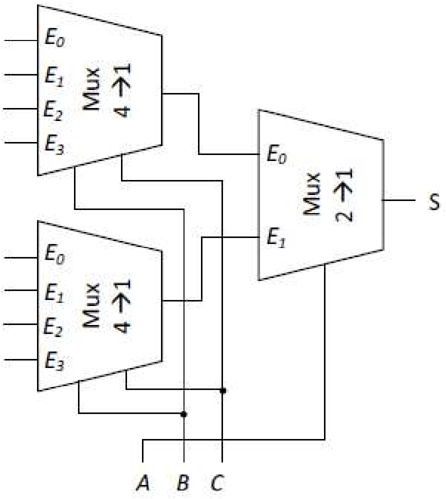
$F(A,B,C) = \overline{A}.\overline{B} + \overline{A}.B.\overline{C} + \overline{B}.\overline{C} + A.\overline{B}.C$

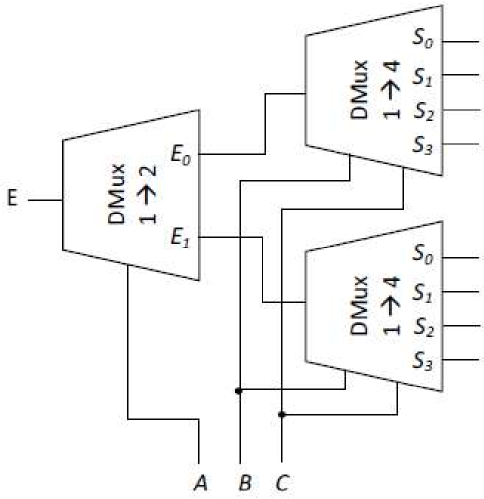


$F(A,B,C,D) = A.B.\overline{D} + A.\overline{B}.C + A.\overline{B}.C.D$



3. Implementation of an 8x1 multiplexer and a 1x8 demultiplexer using 4x1 and 2x1 multiplexers, and 1x4 and 1x2 demultiplexers.

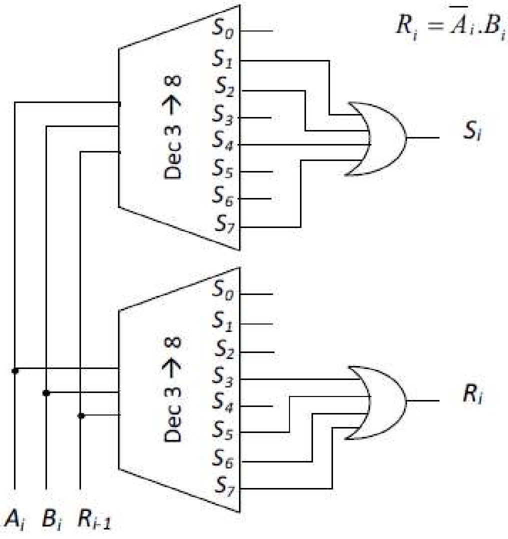




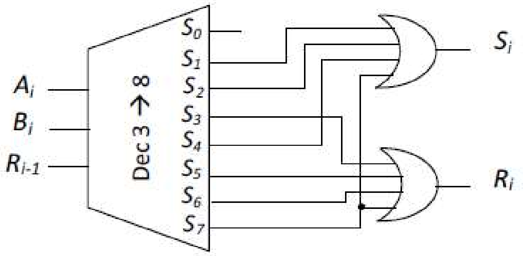
Exercise 7. Logical functions with decoders.

1. Full adder with binary decoders (3x8).

$$S_i = \overline{A}_i.\overline{B}_i.R_{i-1} + \overline{A}_i.B_i.\overline{R}_{i-1} + A_i.\overline{B}_i.\overline{R}_{i-1} + A_i.B_i.R_{i-1}$$
$$R_i = \overline{A}_i.B_i.R_{i-1} + A_i.\overline{B}_i.R_{i-1} + A_i.B_i.\overline{R}_{i-1} + A_i.B_i.R_{i-1}$$

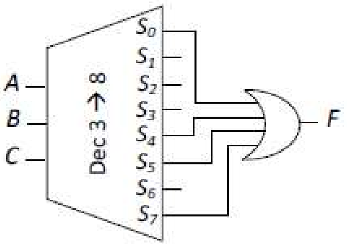


Ou bien

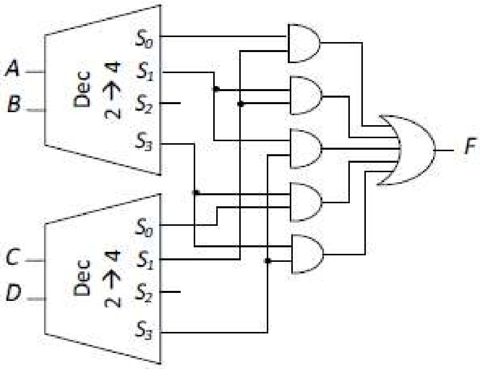


2. Implementation of the following functions using decoders (1x2), (2x4), and (3x8) and logical gates.

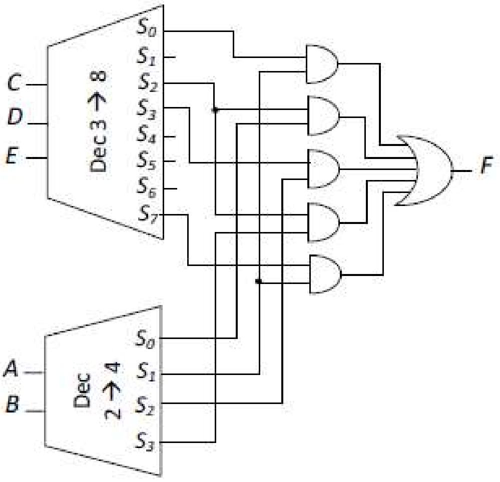
$F(A,B,C)=\sum(0,4,5,7)$



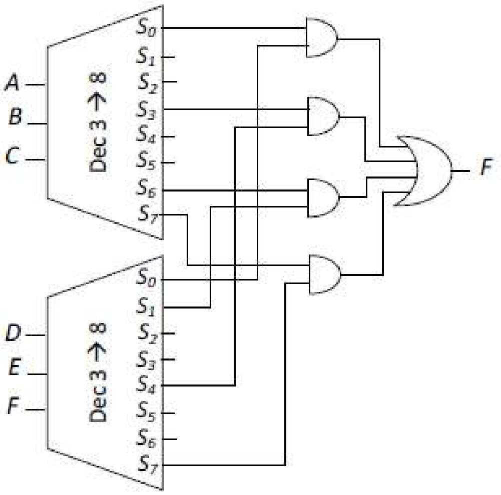
$F(A,B,C,D)=\sum(1,5,7,12,15)$



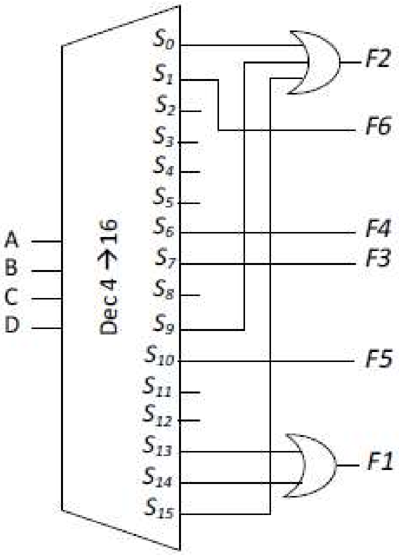
$F(A,B,C,D,E)=\sum(2,8,15,19,26)$



$F(A,B,C,D,E,F)=\sum(0,28,49,63)$



3. Implementation of the following functions using a suitable decoder and logical gates.


A
B
C
D
Dec 4 → 16
S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
F2
F6
F4
F3
F5
F1