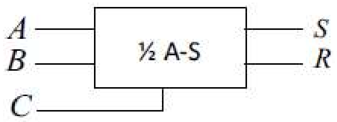
Exercise series N° 2

Exercise 1: Adder/subtractor

1. Using the same steps followed in the course to design the half adder.
Make a circuit that calculates 1-bit by 1-bit subtraction (a half-subtractor).

2. The following figure shows a half-adder/subtractor, which accepts, in addition to inputs A, B and outputs S, R, a control input C indicating the type of operation to execute. The circuit therefore performs an addition on A and B when command C is 0 and a subtraction on A and B when command C is 1.

- Determine the logic equations and draw the logic diagram for this circuit.



3. Based on the half-adder/subtractor from the previous question, design a complete 1-bit by 1-bit adder/subtractor with an input carry.

4. Give the logic diagram of a 4-bit by 4-bit adder/subtractor.

Exercise 2: Multiplier

1. Create a circuit that multiplies 1 bit by 1 bit.
2. Create a 2-bit by 2-bit multiplier following the same steps as in the first question.
3. Create a 2-bit by 2-bit multiplier using the 1-bit by 1-bit multiplier created in the first question and a half-adders.

Exercise 3: Comparator

The following diagram shows a 1-bit by 1-bit comparator which, starting from the two input bits A and B, indicates which of the three output bits E, G and L is greater than the other, as follows.

1) E = 1 if A = B **2)** G = 1 if A > B **3)** L = 1 if A < B

1. Write the logic equations and logic diagram for this circuit.

2. Make a 2-bit comparator using 1-bit comparators and logic gates. (Hint: use one comparator to compare low-order bits and another to compare high-order bits).

3. Deduce the logic diagram of a 3-bit comparator.

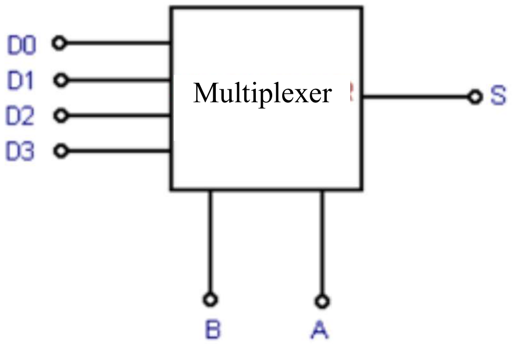
Exercise 04: Logic functions with decoders

A majority function M is a logic function which gives the value 1 when the majority of input values are "1" (Majority: 2 or 3 of the variables are in state 1).

1. Use a decoder (3x8) to implement the majority function for 3 input variables A, B and C.
2. Perform the following function F (A, B, C) =∑(0,4,5,7) using a decoder (3x8) and logic gates.

Exercise 5: Logic functions with multiplexers

A. The assembly shown in figure 1 represents the operating diagram of a four-channel multiplexer. The principle is to have each of the inputs in the output one after the other, in turn.



Let's call the two control signals A and B.

1. What are the possible combinations of A and B.
2. Draw up a truth table implementing the multiplexing function.
3. Produce the corresponding flow chart

B. Perform the function $F(A,B,C)=\overline{A}.B+\overline{B}.C$ using a 4x1 multiplexer.

Additional exercises:

Exercise 1: 7-segment display

7-segment displays are numerical displays made up of segments which can be lit or unlit to display a decimal digit: 0, 1, 2, ... , 9 or letters for hexadecimal: a, b, c, d, e, f.
Each segment is associated with a letter as follows:
For example, to display the number 1, turn on segments B and C:

Write the logic equations and draw the logic diagram of the circuit used to control this type of display.

Exercise 2: Logic functions with multiplexers

1. A majority function M is a logic function which gives the value 1 when the majority of input values are 1.
   (a) Use a multiplexer (16x1) to implement the majority function for 4 input variables A, B, C and D.
   (b) Same question for a majority function with 5 variables A, B, C, D and E.
2. Perform the following functions using a multiplexer (8x1).

$$F(A,B,C)=A.\overline{B}+\overline{A}.\overline{C}+B.\overline{C}$$
$$F(A,B,C)=\overline{A}.\overline{B}+\overline{A}.B.\overline{C}+\overline{B}.\overline{C}+A.\overline{B}.C$$
$$F(A,B,C,D)=A.B.\overline{D}+A.\overline{B}.C+A.\overline{B}.C.D$$

3. Create a multiplexer (8x1) using multiplexers (4x1) and (2x1).
4. Create a demultiplexer (1x8) using demultiplexers (1x4) and (1x2).

Exercise 3: Logic functions with decoders

1. A complete adder can be made using binary decoders (3x8). Make this circuit and give the corresponding logic diagram.

2. Perform the following functions using only decoders (1x2), (2x4) and (3x8) and logic gates.

$$F(A,B,C)=\sum(0,4,5,7) \qquad F(A,B,C,D,E)=\sum(2,8,15,19,26)$$
$$F(A,B,C,D)=\sum(1,5,7,12,15) \qquad F(A,B,C,D,E,F)=\sum(0,28,49,63)$$

3. Use a suitable decoder to perform the following functions.

$$F_1=A.B.C.\overline{D}+A.B.C.\overline{D} \qquad F_3=\overline{A}.B.C.D \qquad F_5=A.\overline{B}.C.\overline{D}$$
$$F_2=\overline{A}.\overline{B}.\overline{C}.\overline{D}+A.B.C.D+A.B.\overline{C}.\overline{D} \qquad F_4=\overline{A}.B.C.\overline{D} \qquad F_6=\overline{A}.\overline{B}.\overline{C}.D$$